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32

SH7619 CPU Board

M3A-HS19

User's Manual

Renesas 32-Bit RISC Microcomputers
SuperH™ RISC engine Family/SH7619 Group

User's Manual

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Chapter1
Overview

1.1 Overview

The M3A-HS19 is a CPU board designed to evaluate the feature and performance of the SH7619 Group of Renesas Technology original MCU, as well as developing and evaluating the application software for the MCUs.

SH7619 data bus, address bus and on-chip peripheral pins are all connected to expansion connectors and appropriate connectors to allow for the timing evaluation with peripherals using measurement instruments, and the development of the optional boards according to its application. Furthermore, it can be connected with an RS-232C connector and a LAN connector, and a PC card can be mounted on the board.

Renesas Technology E10A-USB on-chip emulator can also be connected to the M3A-HS19.

1.2 Configuration

Figure 1.2.1 shows an example of system configuration using the M3A-HS19.

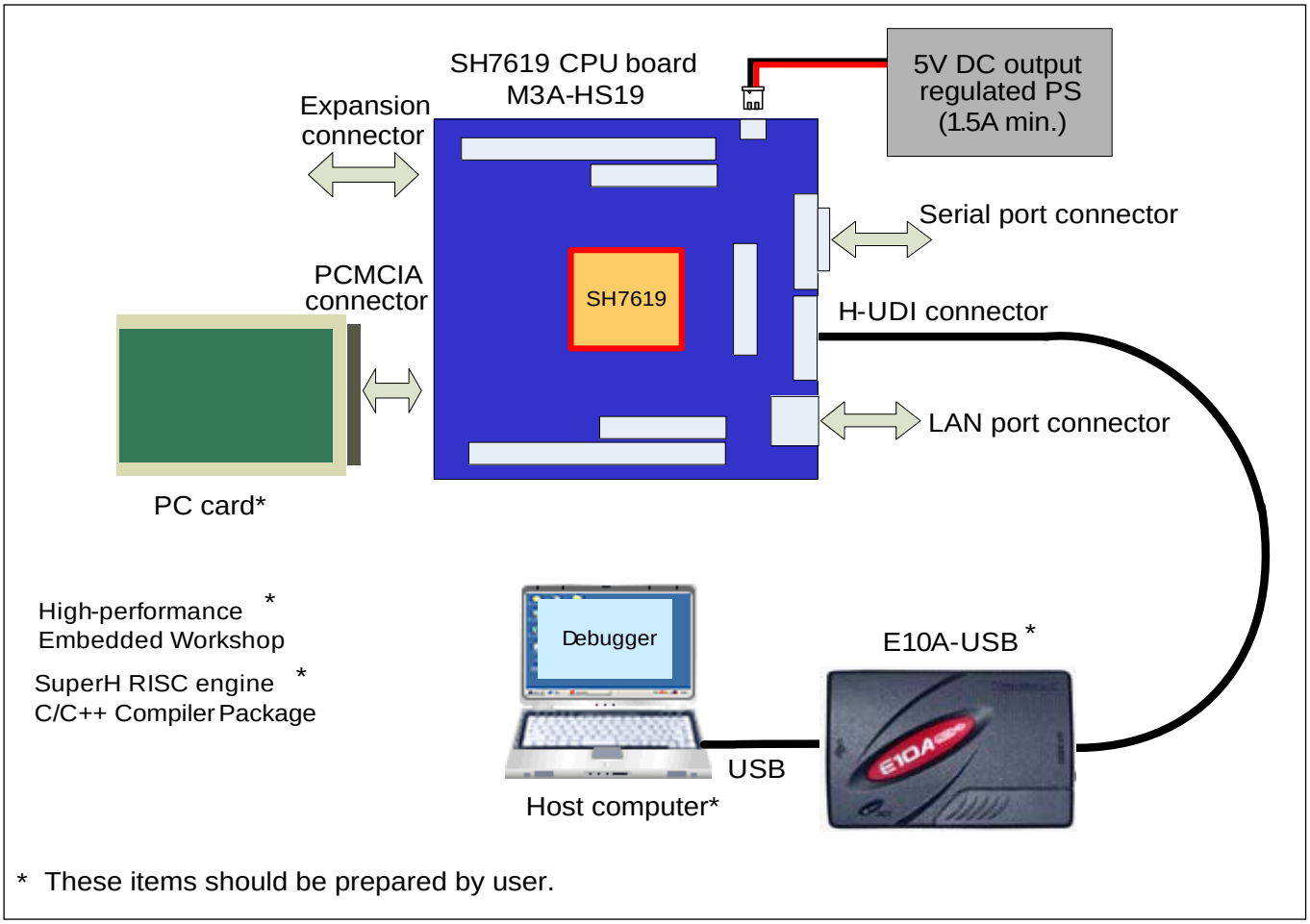

Figure 1.2.1 M3A-HS19 System Configuration

1.3 External Specifications

Table 1.3.1 lists external specifications.

Table 1.3.1 External Specifications

No.	Items	Description
1	CPU	SH7619 ● Input (XIN) clock: 15.625 MHz ● Bus clock: 62.5 MHz at maximum ● CPU clock: 125 MHz at maximum
2	Memories	● SDRAM (16-bit data bus) • EDS1216AATA-75E: 1 (16 MB) ● Flash memory (16-bit data bus) • S29GL032A90TFIR4: 1 (4 MB) ● EEPROM (Serial) • S93C76AFT-V-G: 1 (8 KB, 512 x 16)
3	Connectors	● Expansion Connector (Bus, I/O, VCC, GND: 140 pins in total: Through-hole) ● Channel 1 serial port connector (2-pin: Through-hole) ● Channel 2 serial port connector (D-sub 9-pin) ● RS-422 serial connector (4-pin: Through-hole) ● RJ-45 LAN connector (8-pin, RJ-45) ● PC card connector (68-pin) ● H-UDI connector (14-pin) ● Power connector (2-pin: 5 V) ● External power connector (2-pin: 1.8 V: Through-hole)
4	LEDs	● Power LED: 1 ● User LEDs: 4
5	Switches	● Power switch: 1 ● Reset push-button switch: 1 ● NMI push-button switch: 1 ● IRQ0 push-button switch: 1 ● User DIP switches: 4/package ● Mode DIP switches: 4/package ● 1.8 V external switch jumper: 1 ● PCMCIA power switch jumper: 1 ● PCMCIA bus switch enable jumper: 1 ● Expansion connector signal select jumpers: 5
6	Dimensions	● Dimensions: 100 mm x 100 mm ● Mounting form:6 layers, double-sided ● Board configuration:1 board

1.4 Appearance

Figure 1.4.1 shows the appearance of the M3A-HS19.

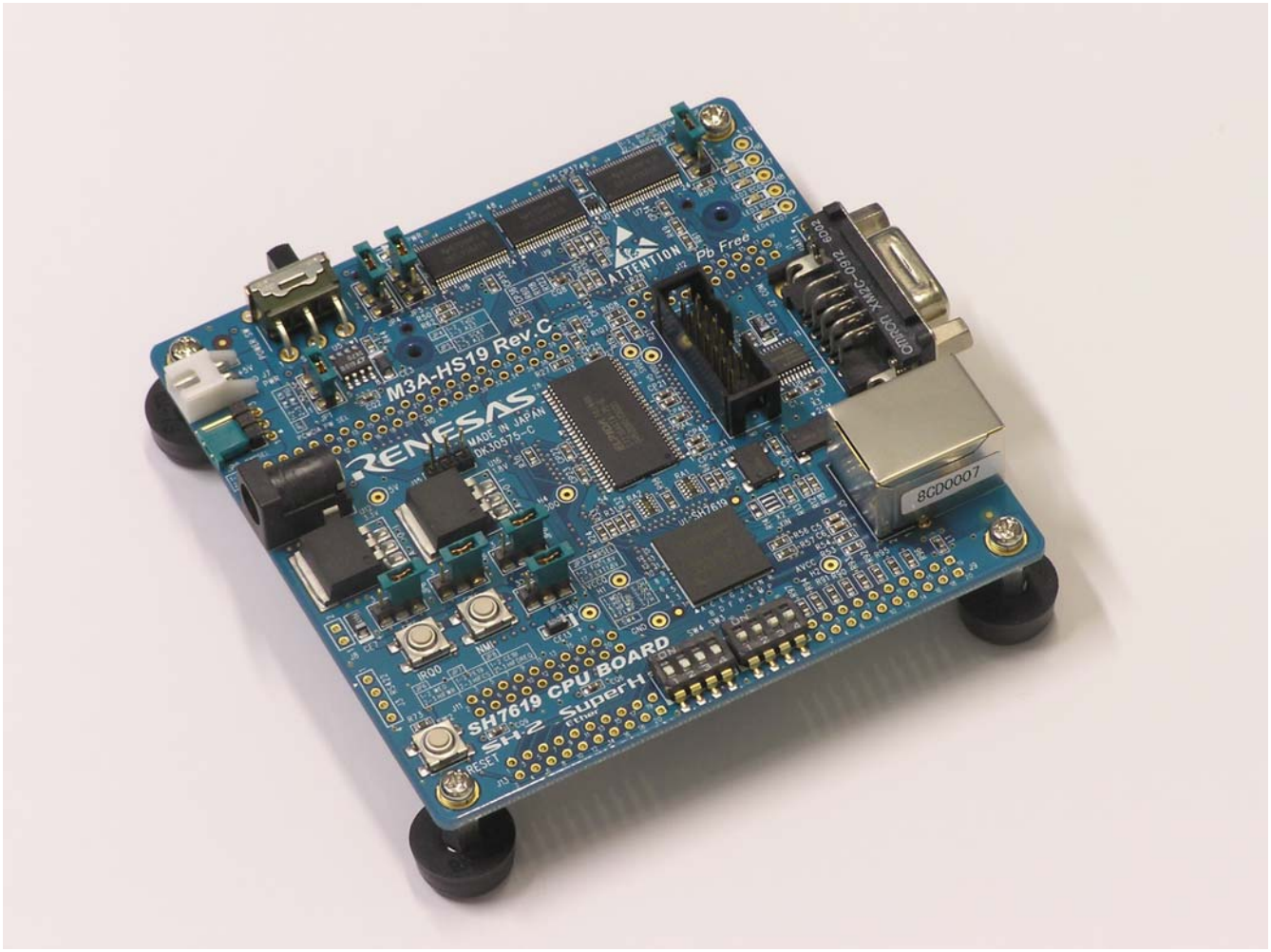

Figure 1.4.1 M3A-HS19 Appearance

1.5 M3A-HS19 Block Diagrams

Figure 1.5.1 shows the system block diagram.

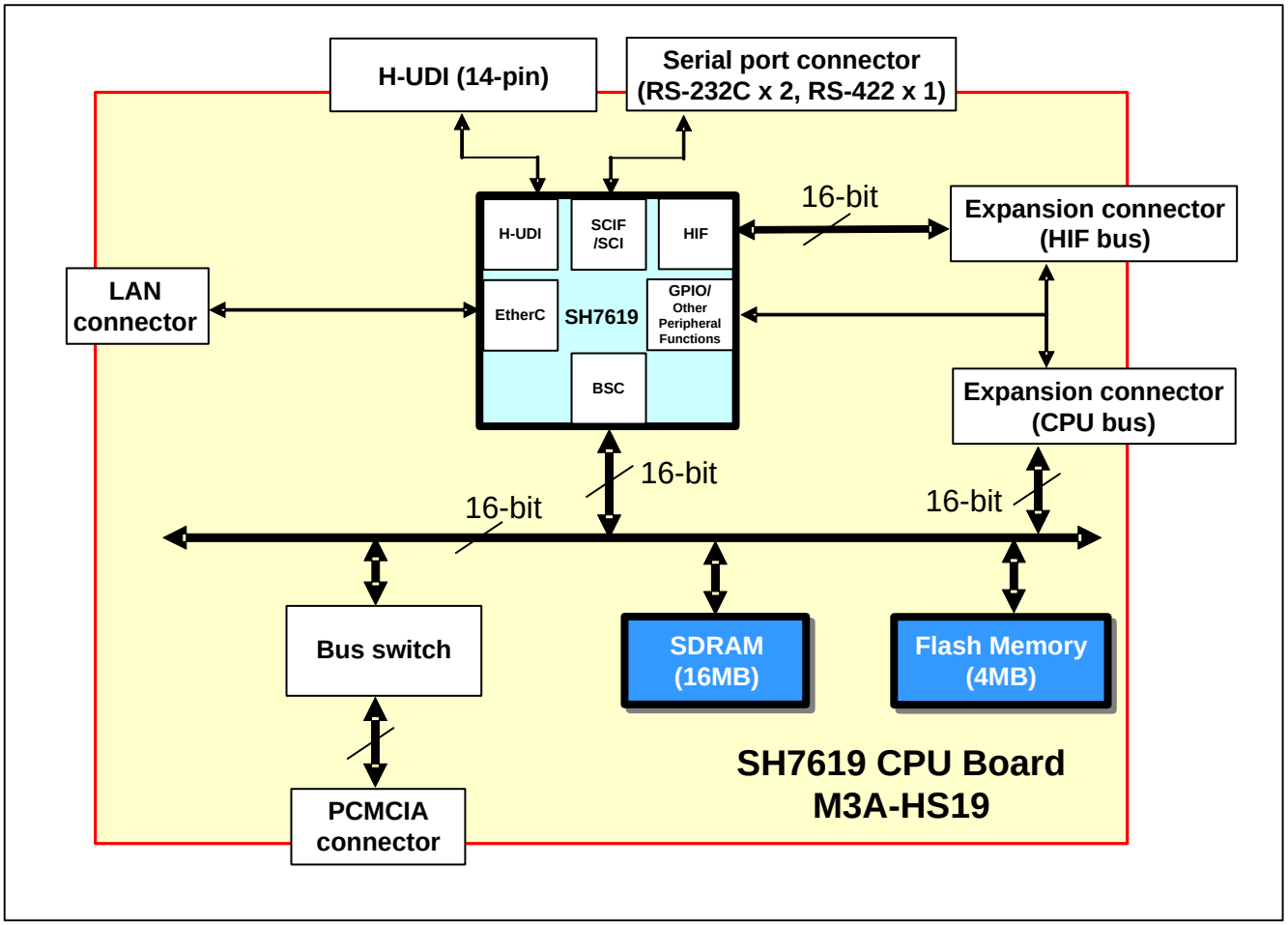

Figure 1.5.1 System Block Diagram

1.6 M3A-HS19 Board Overview

Figure 1.6.1 shows the M3A-HS19 board overview.

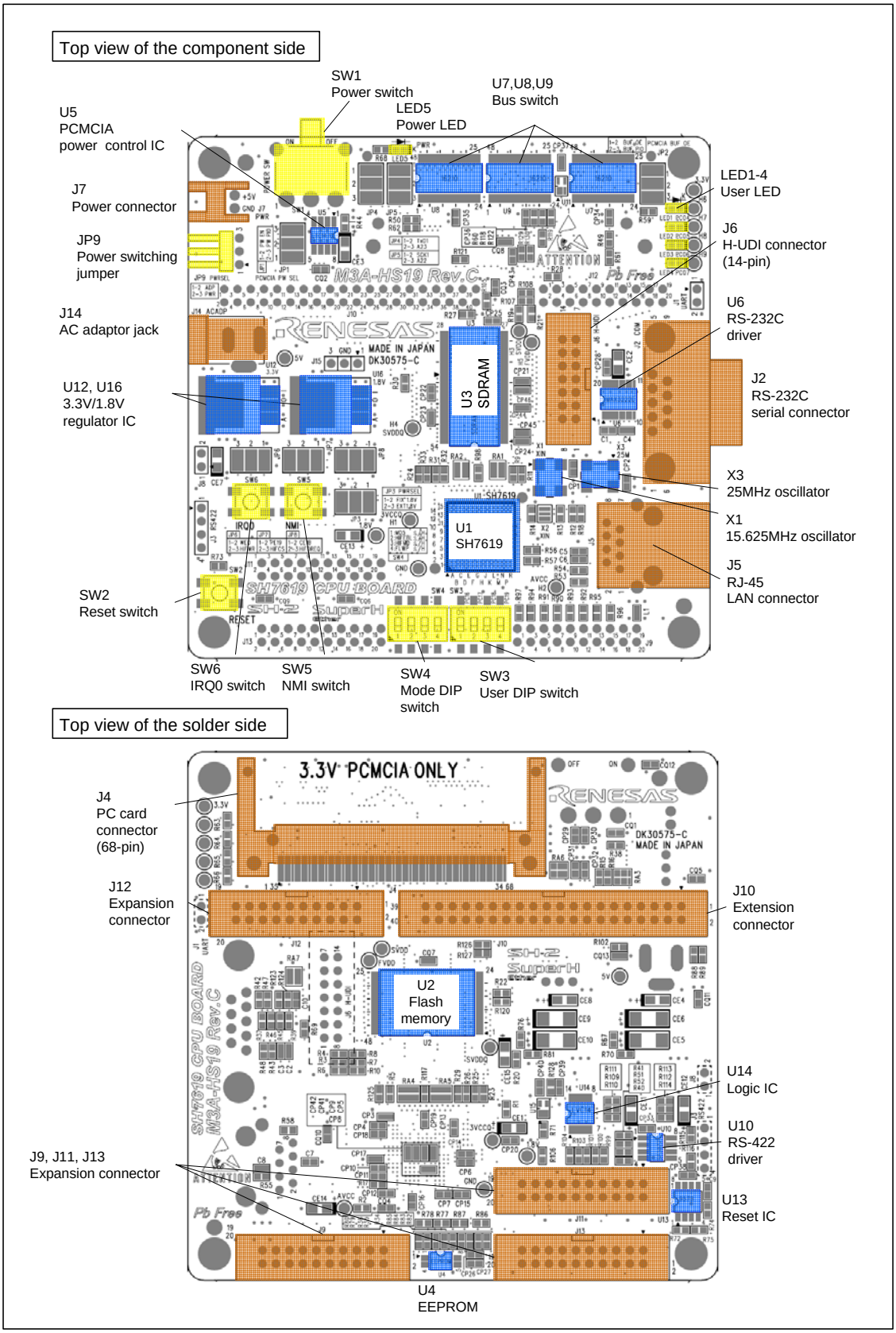

Figure 1.6.1 M3A-HS19 Board External View

Table 1.6.1 lists major components mounted on the M3A-HS19

Table 1.6.1 Major Components

Part Number	Name	Remarks (By manufacturer)	Recommended Optional Parts (By manufacturer)
U1	CPU	R4S76190W125BGV (Renesas)	
U2	Flash memory	S29GL032A90TFIR4 (Spansion)	
U3	SDRAM	EDS1216AATA-75E (Elpida)	
U4	EEPROM	S93C76AFT-V-G (SII)	
U5	PCMCIA power control IC	LTC1470CS8#PBF (Linear)	
U6	RS-232C driver	SP3222ECY (Sipex)	
U7,U8,U9	Bus switch	SN74CBTLV16210GR (TI)	
U10	RS-422 driver	SP3077EEN-L (Sipex)	
U11,U15	Logic IC	TC7S08FU (TOSHIBA)	
U12,U16	Regulator IC	LMS1587CSX-ADJ (NS)	
U13	Reset IC	M51957BFP (Renesas)	
U14	Logic IC	SN74LVC14APWR (TI)	
X1	Oscillator	SG-8002JF_15.625 MHz (Epson)	
X2	Ceramic resonator	Optional, 15.625 MHz	CSTCE15M7 (Murata)
X3	Oscillator	SG-8002JF_25.000 MHz (Epson)	
J1	Serial port connector (Ch1)	Optional, 2-pin MIL standard connector	A2-2PA-2.54DSA (Hirose)
J2	Serial port connector (Ch2)	XM2C-0912-112 (OMRON)	
J3	RS-422 serial connector	Optional	A2-4PA-2.54DSA (Hirose)
J4	PC card connector	ICM-C68H-S112-400R1 (J.S.T.)	
J5	RJ-45 LAN connector	TLA-6T718 (TDK)	
J6	H-UDI connector	7614-6002 (Sumitomo 3M)	
J7	Power supply connector	S2B-XH-A (J.S.T.)	
J8	1.8 V External power supply connector	Optional, 2-pin MIL standard connector	A2-2PA-2.54DSA (Hirose)
J9,J11-J13	Expansion connector	Optional, 20-pin MIL pitch connector	XG4C-2031 (OMRON)
J10	Expansion connector	Optional, 40-pin MIL pitch connector	XG4C-4031 (OMRON)
J14	AC adapter jack	HEC0470-01-630 (Hoshiden)	
J15	3-pin connector	XG8V-0331 (OMRON)	
JP1-8	Jumper	HW-3P-G (MAC8)	
JP9	Jumper	XG8V-0334 (OMRON)	
LED1-4	User LED	Yellow, SML-311YT (ROHM)	
LED5	Power LED	Blue, UB1114C (STANLEY)	
SW1	Power switch	MS-12AAH1 (Nikkai)	
SW2	Reset switch (MRES)	B3SN-3012 (OMRON)	
SW3	User DIP switch	A6S-4104-H (OMRON)	
SW4	Mode DIP switch	A6S-4101-H (OMRON)	
SW5	NMI switch	B3SN-3012 (OMRON)	
SW6	IRQ0 switch	B3SN-3012 (OMRON)	

1.7 M3A-HS19 Memory Mapping

Area 0 bus width:	(Default)	MD3 = 0	・・・16-bit
Data alignment:	(SW4-1)	MD5 = 0(ON)	・・・Big endian
		MD5 = 1(OFF)	・・・Little endian

Figure 1.7.1 show the memory mapping examples of the SH7619 on the M3A-HS19.

Logical Address [31~29]	Area	Cacheable/Non-cacheable
000~011	P0	Cacheable
100~	P1	Cacheable
101~	P2	Non cacheable
110~	P3	Cacheable
111~	P4	Non-cacheable (on-chip I/O) etc.

(P0 and shadow area (P1, P2, P3))

Address [28~0]	Area	MAP = 0	MAP = 1
H'0000 0000	Area 0 64 MB	Flash Memory (4 MB) H'0000 0000~H'003F FFFF	Flash Memory (4 MB) H'0000 0000~H'003F FFFF
		User Area	User Area
H'0400 0000	Area 1 64 MB	Reserved * (Do not use)	Reserved * (Do not use)
H'0800 0000	Area 2 64 MB	Reserved * (Do not use)	Reserved * (Do not use)
H'0C00 0000	Area 3 64 MB	SDRAM (16 MB) H'0C00 0000~H'0CFF FFFF	SDRAM (16 MB) H'0C00 0000~H'0CFF FFFF
		User Area	User Area
H'1000 0000	Area 4 64 MB	User Area	User Area
H'1400 0000	Area 5A 32 MB	Reserved (Do not use)	User Area PCMCIA
H'1600 0000	Area 5B 32 MB	User Area	
H'1800 0000	Area 6A 32 MB	Reserved (Do not use)	User Area PCMCIA
H'1A00 0000	Area 6B 32 MB	User Area	
H'1C00 0000 H'1FFF FFFF	Area 7 64 MB	Reserved * (Do not use)	Reserved (Do not use)

Note: H'0000 0000 to H'1FFF FFFF are the cache-enabled area.

Figure 1.7.1 SH7619 Memory Mapping Examples

1.8 Absolute Maximum Ratings

Table 1.8.1 lists the absolute maximum ratings.

Table 1.8.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Remarks
VCC	5 V system power supply voltage	-0.3 to 6.0 V	Relative to VSS
3VCC	3.3 V system power supply voltage	-0.3 to 3.8 V	Relative to VSS
1.8VCC	1.8 V system power supply voltage	-0.3 to 2.1 V	Relative to VSS
Topr	Operating temperature	-5 to 55°C	No condensation, no corrosion gas allowed.
Tstr	Storage temperature	-10 to 60°C	No condensation, no corrosion gas allowed.

Note: Temperature refers to the air temperature in the vicinity of the board.

1.9 Recommended Operating Conditions

Table 1.9.1 lists the recommended operating conditions.

Table 1.9.1 Recommended Operating Conditions

Symbol	Parameter	Value	Remarks
VCC	5 V power supply voltage	4.75 to 5.25 V	Relative to VSS
3VCC	3.3 V power supply voltage	3.0 to 3.6 V	Relative to VSS (Always supplied by regulator)
1.8VCC	1.8 V power supply voltage	1.71 to 1.89 V	Relative to VSS (Normally supplied by regulator)
-	Maximum current consumption on the board	1 A max.	
Topr	Operating temperature	0 to 50°C	No condensation, no corrosion gas allowed.

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Chapter2
Features and Specifications

2.1 Features

Table 2.1.1 lists the functional modules.

Table 2.1.1 Functional Modules

Section	Features	Description
2.2	CPU	SH7619, clock mode 1 ● Input (XIN) clock: 15.625 MHz ● Bus clock: 62.5 MHz, max. ● CPU clock: 125 MHz, max.
2.3	Memories	● U Memory (CPU) • 16-KB memory ● Flash Memory • S29GL032A90TFIR4: 1 (4 MB) ● SDRAM • EDS1216AATA-75E: 1 (16 MB) ● EEPROM • S-93C76AFT-V-G: 1 (8 KB, 512 x 16)
2.4	Serial Port Interface	Connects SCIF2 of the SH7619 to a serial port connector
2.5	PCMCIA Card Interface	Connects PCMCIA control signal and bus of the SH7619 to the PCMCIA connector
2.6	LAN Port Interface	Connects the SH7619 Ether I/O to an RJ-45 connector
2.7	I/O Ports	Connects the SH7619 I/O port to an expansion connector
2.8	Power Supply Circuit	Controls the system power supply of the M3A-HS19
2.9	Clock Module	Controls the clock
2.10	Reset Module	Reset control of device mounted on the M3A-HS19
2.11	Interrupt Switches	Connects to the NMI pin and IRQ0 pin
2.12	E10A-USB Interface	SH7619 H-UDI/AUD interface
-	Operational specifications	Connectors, switches, jumpers, LEDs ● Expansion connector, H-UDI connector ● PCMCIA, ETHER, RS-232C connector ● Switches and LEDs Refer to Chapter 3 for details

2.2 CPU

2.2.1 SH7619

The M3A-HS19 CPU board includes the SH7619, the 32-bit RISC MCU operates with a maximum frequency of 125 MHz. The SH7619 is equipped with an Ethernet controller that includes an IEEE802.3u compliant Media Access Controller and a Physical Layer Transceiver. Moreover, the SH7619 has both a 16-KB U memory (RAM) and a 16-KB instruction/data unified cache memory. These on-chip modules enable the SH7619 to be used in a wide range of applications from data processing to control equipments.

The M3A-HS19 can be operated at a maximum frequency of 125 MHz (external bus: 62.5 MHz, max) using a 15.625 MHz input clock. The dedicated clock of 25.000 MHz input from CK_PHY pin is used as an on-chip PHY clock.

Figure 2.2.1 shows the SH7619 pin assignments.

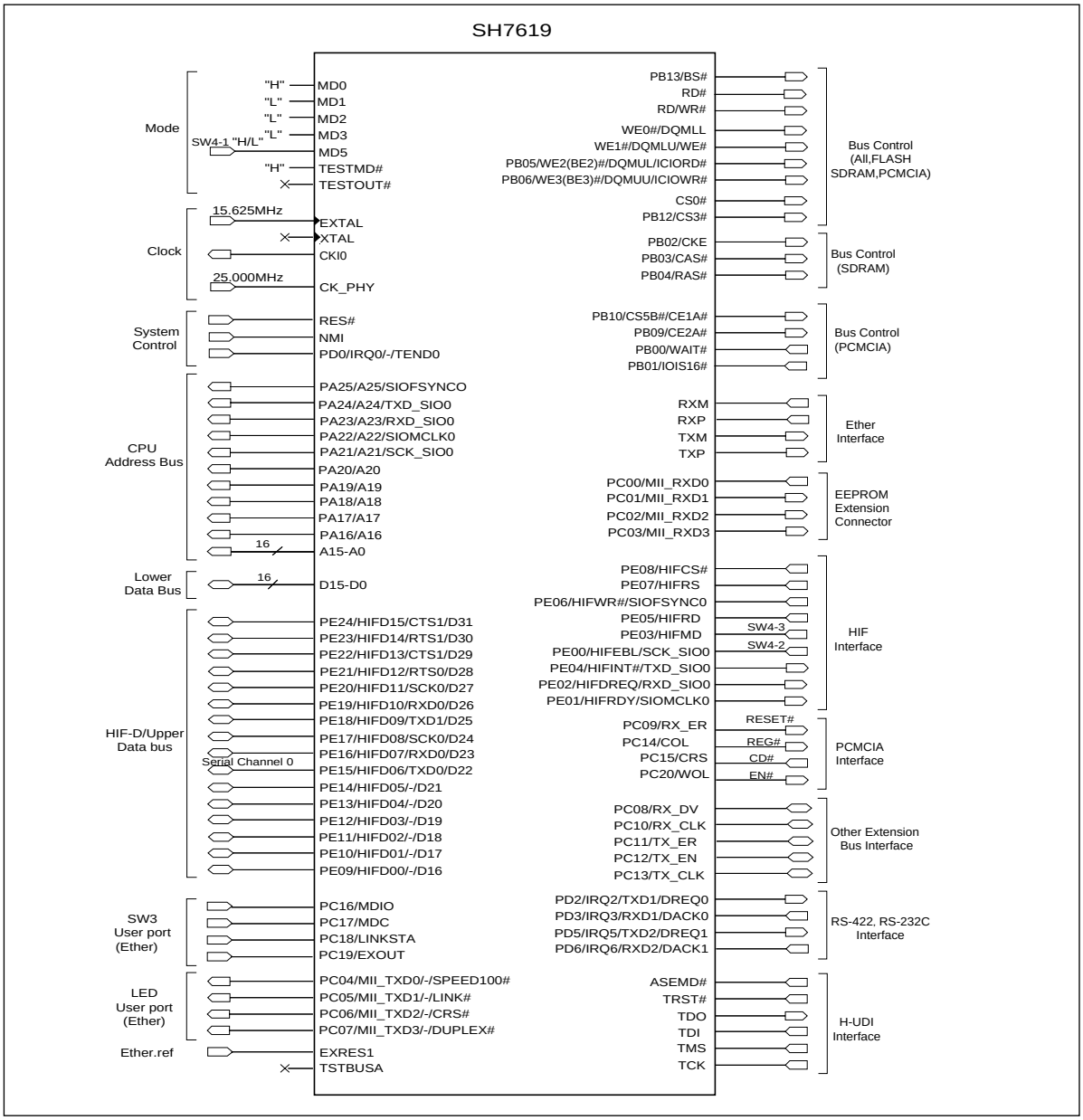

Figure 2.2.1 Pin Assignments by function

2.3 Memory

The M3A-HS19 includes the SH7619 on-chip U memory, an external flash memory, external SDRAM and EEPROM. Details are described below (Except the PC card).

2.3.1 SH7619 U Memory and Cache Memory

The SH7619 has a 16-KB (RAM) U memory module (address: H'E55FC000~H'E55FFFFF) and a 16-KB instruction/data-unified cache memory.

2.3.2 Flash Memory S29GL032A90TFIR4 (Standard component)

The M3A-HS19 comes standard with a flash memory listed in Table 2.3.1 to store a user program.
The flash memory is an external bus 16-bit mode fixed and operates at 3.3 V single. The write-protection of flash memory can be enabled or disabled by DIP switches (SW4-4).
Figure 2.3.1 shows the Flash Memory Block Diagram. Table 2.3.2 lists setting examples of the bus state controller(write/read) when the SH7619 bus clock operates at 62.5 MHz (clock mode 1), and Figure 2.3.2 shows read and write access timing example.

Table 2.3.1 Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
S29GL032A90TFIR4	16-bit mode	4 MB (16 bits x 2 Mwords x 1)	90 ns

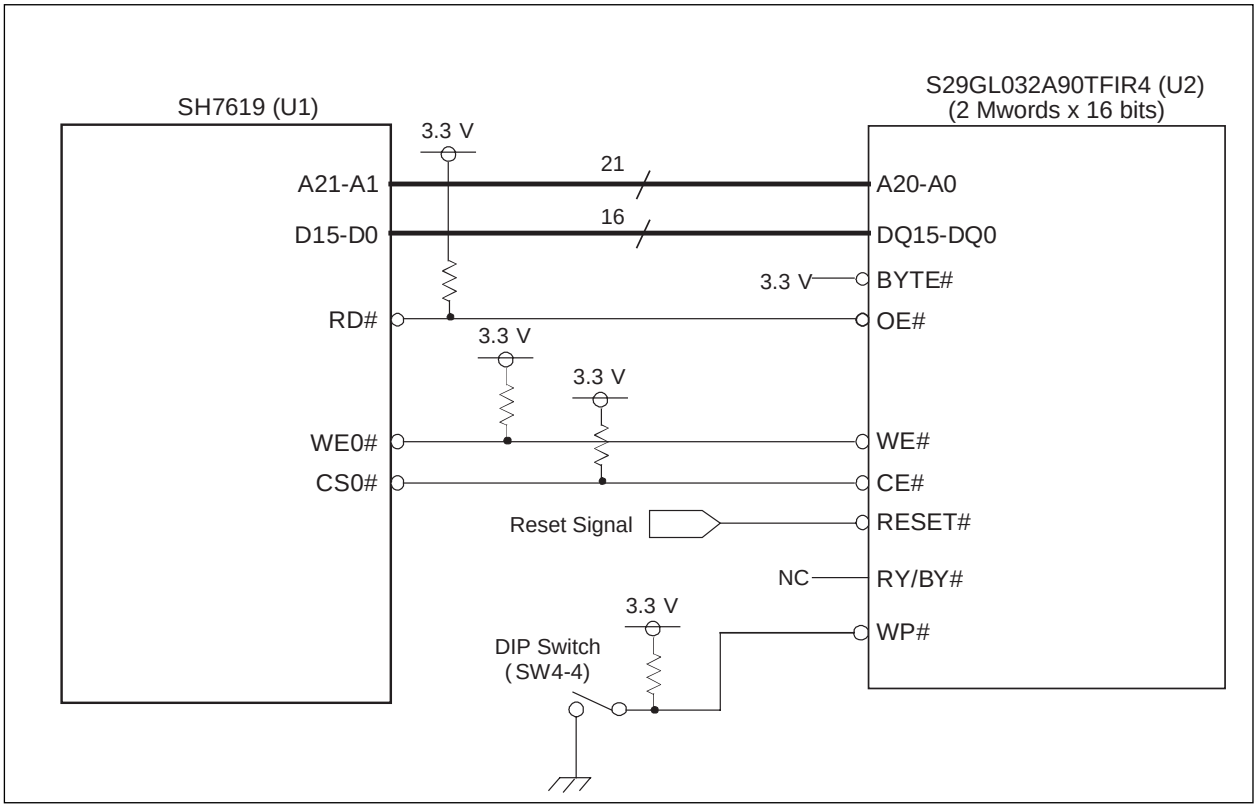

Figure 2.3.1 Flash Memory Block Diagram

Table 2.3.2 Setting Example of Bus State Controller (Flash Memory Write and Read)

User Area	Applicable Device	Settings for Bus State Controller
CS0	S29GL032A90TFIR4	CS0 Space Bus Control Register: CS0BCR Initial value: H'36DB 0400 (MD3 = "L") Recommended value: H'1000 0400 • Idle Cycles between Write-Read Cycles and Write-Write Cycles IWW[1:0] = B'01: 1 idle cycle inserted • Data bus width BSZ[1:0] = B'10: *Shall be ignored. CS0 space wait control register: CS0WCR Initial value: H'0000 0500 Recommended value: H'0000 0AC1 • Number of Delay Cycles from address, CS0# Assertion to RD#, WEn# SW[1:0] = B'01; 1.5 cycles • Number of Access Wait Cycles WR[3:0] = B'0101; 5 cycles • Ignore external WAIT input WM = B'1; • Number of Delay Cycles from RD#, WEn# negation to address, CS0# negation HW[1:0] = B'01; 1.5 cycles

<Write/Read Timing>

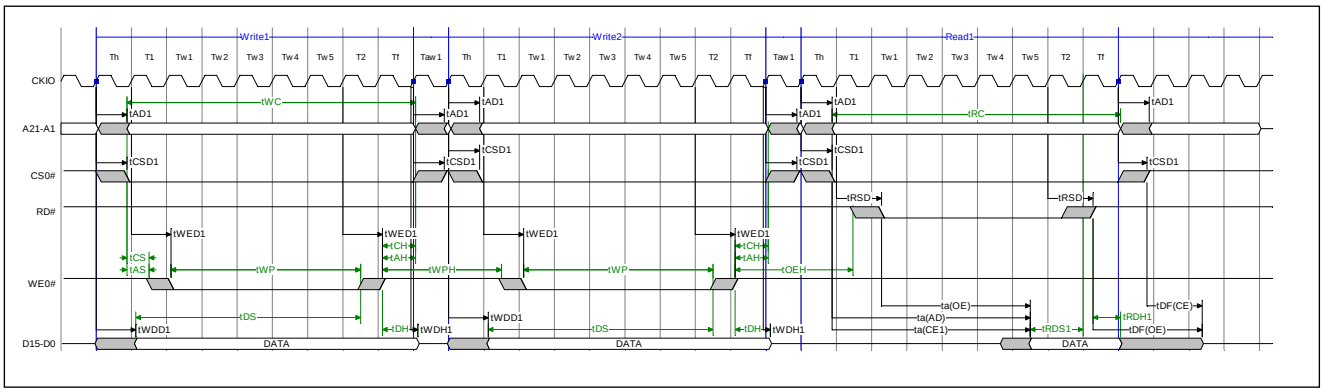

Figure 2.3.2 Flash Memory Read and Write Access Timing Example

2.3.3 External Synchronous DRAM (SDRAM)

The M3A-HS19 is provided with a 16-MB synchronous DRAM (SDRAM) as an external main memory. The SDRAM is controlled by the SH7619 on-chip bus state controller. The SDRAM is accessed in 16-bit bus.
Table 2.3.3 lists SDRAM specifications used on the M3A-HS19, and Figure 2.3.3 shows its block diagram.

Table 2.3.3 SDRAM Specifications

Items	Description
Part Number	EDS1216AATA-75E
Configuration	16 MB (16-bit bus width) x 1
Capacity	16 MB
Access Time	5.4 ns
CAS Latency	2 (at 62.5 MHz bus clock)
Refresh Interval	4,096 refresh cycles in every 64 ms
Row Address	A11- A0
Column Address	A8 - A0
Number of Banks	4-banks controlled by BA0, BA1

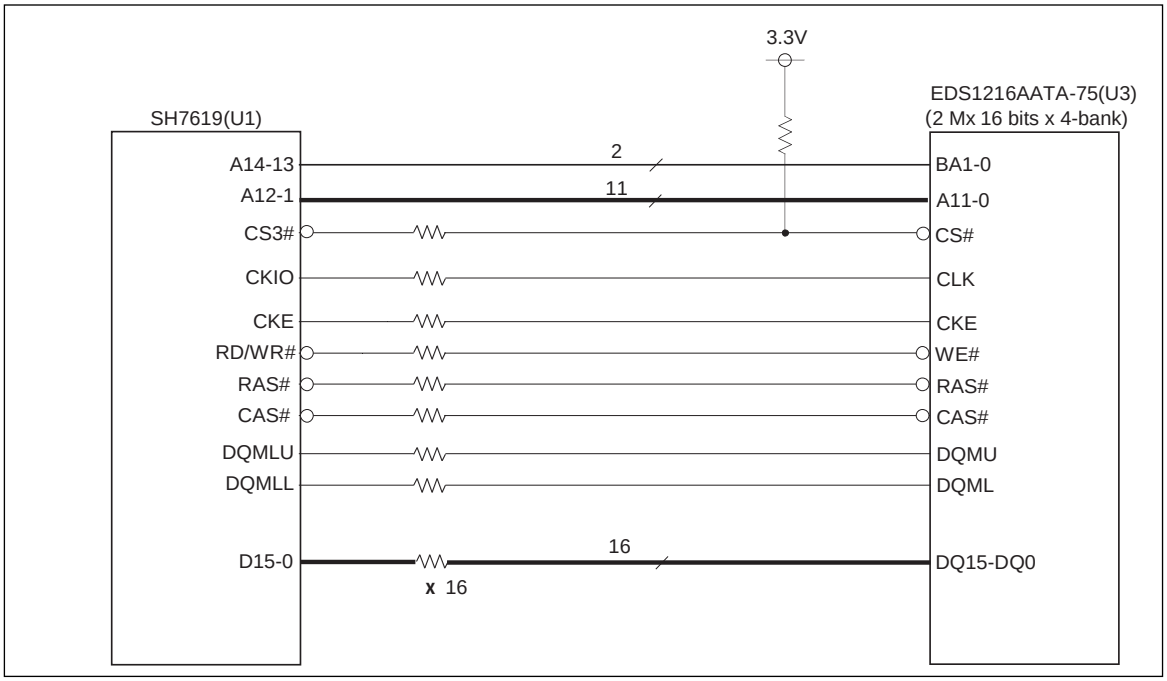

Figure 2.3.3 External SDRAM Block Diagram

A power-on sequence is required to use a SDRAM. Power-on sequence is to initialize the pin function controller (PFC), set registers in the bus state controller and write data in the SDRAM mode register.

Table 2.3.4 lists the access address when writing in the SDRAM mode register on the CS3 space.

Table 2.3.4 Access Address for SDRAM Mode Register Write (CS3 Space)

Data bus width	CAS latency	Burst read/single write (burst length 1)		Burst read/burst write (burst length 1)	
		Access Address	External Address Pin	Access Address	External Address Pin
16 bits	2	H'F8FD 5440	H'0000 0440	H'F8FD 5040	H'0000 0040

Execute following settings to the M3A-HS19 SDRAM mode register.

• Burst length: Burst read/single write (burst length 1)

• Wrap type: Sequential

• CAS latency: 2 cycles

To write data in the SDRAM mode register as shown in Table 2.3.4, write the arbitrary data in words to the address of H'F8FD 5440 (the data in this case is ignored). Following commands are sequentially issued to the SDRAM by the word writing.

1.All banks precharge command (PALL)

Idle cycles (Tpw), of which number is specified by bits WTRP1 and WTRP0 in CS3WCR, are inserted between the PALL and the first REF commands.

2. Auto-refreshing command (REF) for eight times

Idle cycles (Trc), of which number is specified by bits WTRP1 and WTRP0 in CS3WCR are inserted after issuing REF command

3. Mode register write command (MRS)

Figure 2.3.4 shows a timing example of SDRAM mode register writing.

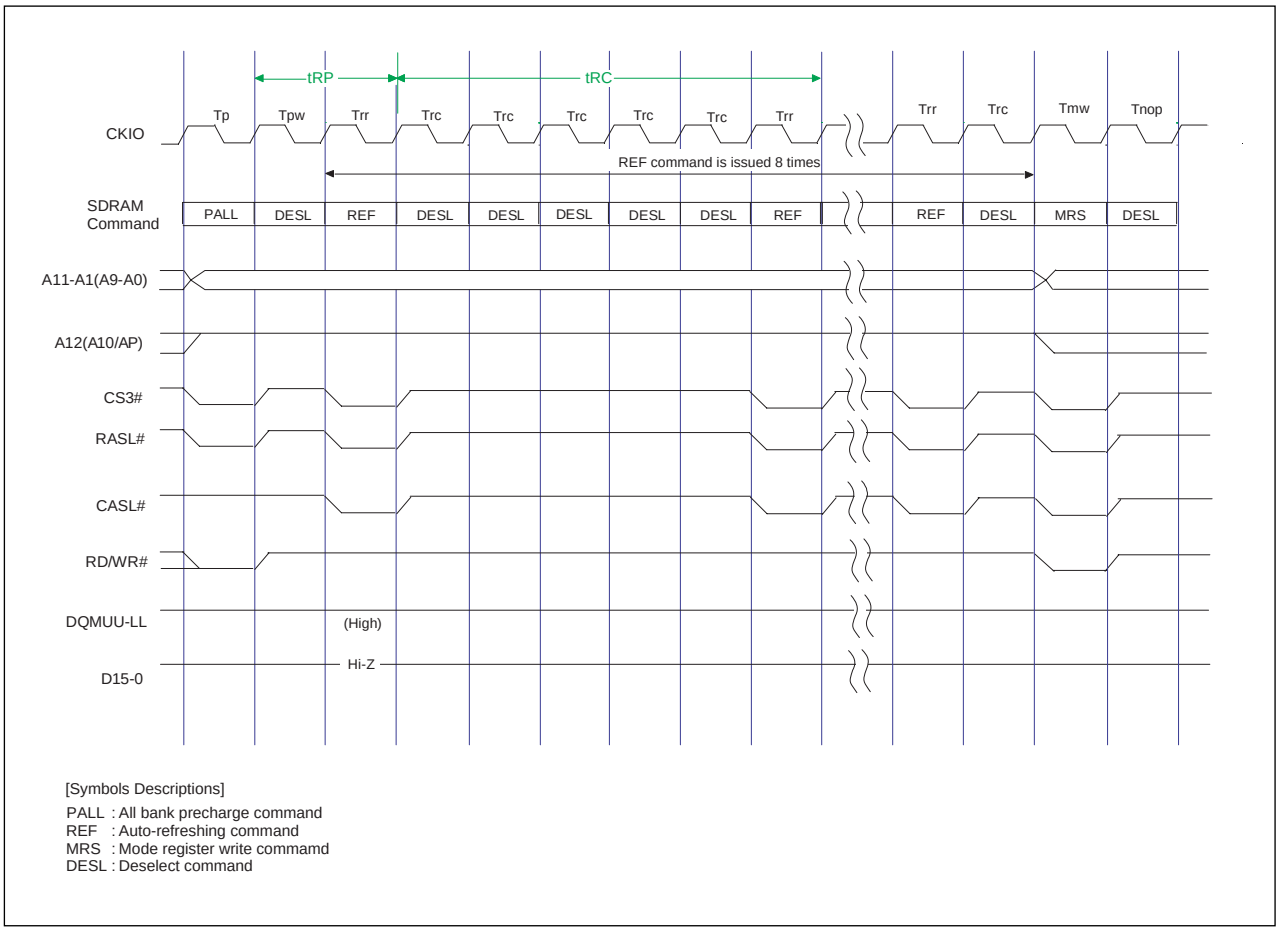

Figure 2.3.4 Timing Example of SDRAM Mode Register Writing

Table2.3.5 lists setting examples of the bus state controller with SH7619 bus clock at 62.5 MHz.

Figure 2.3.5 shows the SDRAM single read/write timing example.

Table2.3.5 Setting Example of Bus State Controller (SDRAM Read/Write)

User Area	Applicable Device	Settings for Bus State Controller
CS3	EDS1216AATA-75E	CS3 Space Bus Control Register: CS3BCR Initial value: H'36DB 0600 Recommended value: H'0000 4400 (in 16-bit bus width) • Memory specification TYPE[3:0] = B'0100; SDRAM • Data bus specification BSZ[1:0] = B'10; 16-bit bus width CS3 Space Wait Control Register: CS3WCR Initial value: H'0000 0500, recommended value: H'0000 2892 • Wait Cycle Number for Precharge Completion WTRP[1:0] = B'01; 1 cycle • Wait Cycle Number from ACTV command to READA WRITA command WTRCD[1:0] = B'10; 2 cycles • Cas Latency for Area 3 A3CL[1:0] = B'01; 2 cycles • Wait Cycle Number for Precharge Start Wait TRWL[1:0] = B'10; 2 cycles • Idle Cycle Number from REF/Self-Refreshing Release to ACTV/REF/MRS Command WTRC[1:0] = B'10; 5 cycles SDRAM Control Register: SDCR Initial value: H'0000 0000, Recommended value: H'0000 0809 • Refresh Control RFSH = B'1; Refreshing is performed • Refresh Control RMODE = B'0; Auto-Refreshing is not performed • Bank active mode BACTV = B'0; Auto-precharge mode • Number of Bits of Row Address for Area 3 A3ROW[1:0] = B'01; 12 bits • Number of Bits of Column Address for Area 3 A3COL[1:0] = B'01; 9 bits Refresh Timer Control / Status Register: RTCSR Initial value: H'0000 0000, Recommended value: H'A55A 0010 • Clock Select CKS[2:0] = B'010; Bϕ/16 • Refresh Count RRC[2:0] = B'000 ; Once Refresh Time Constant Register: RTCOR Initial value: H'0000 0000, Recommended value: H'A55A 003D *The refresh request interval when clock select is set to Bϕ/16 is as follows. 1 cycle: 256 nsec (62.5 MHz/16 = 3.90625 MHz) Refresh request interval in this SDRAM: 15.625 μsec/time 15.625 usec/256 nsec = 61 (0x3D) cycles/refresh counts

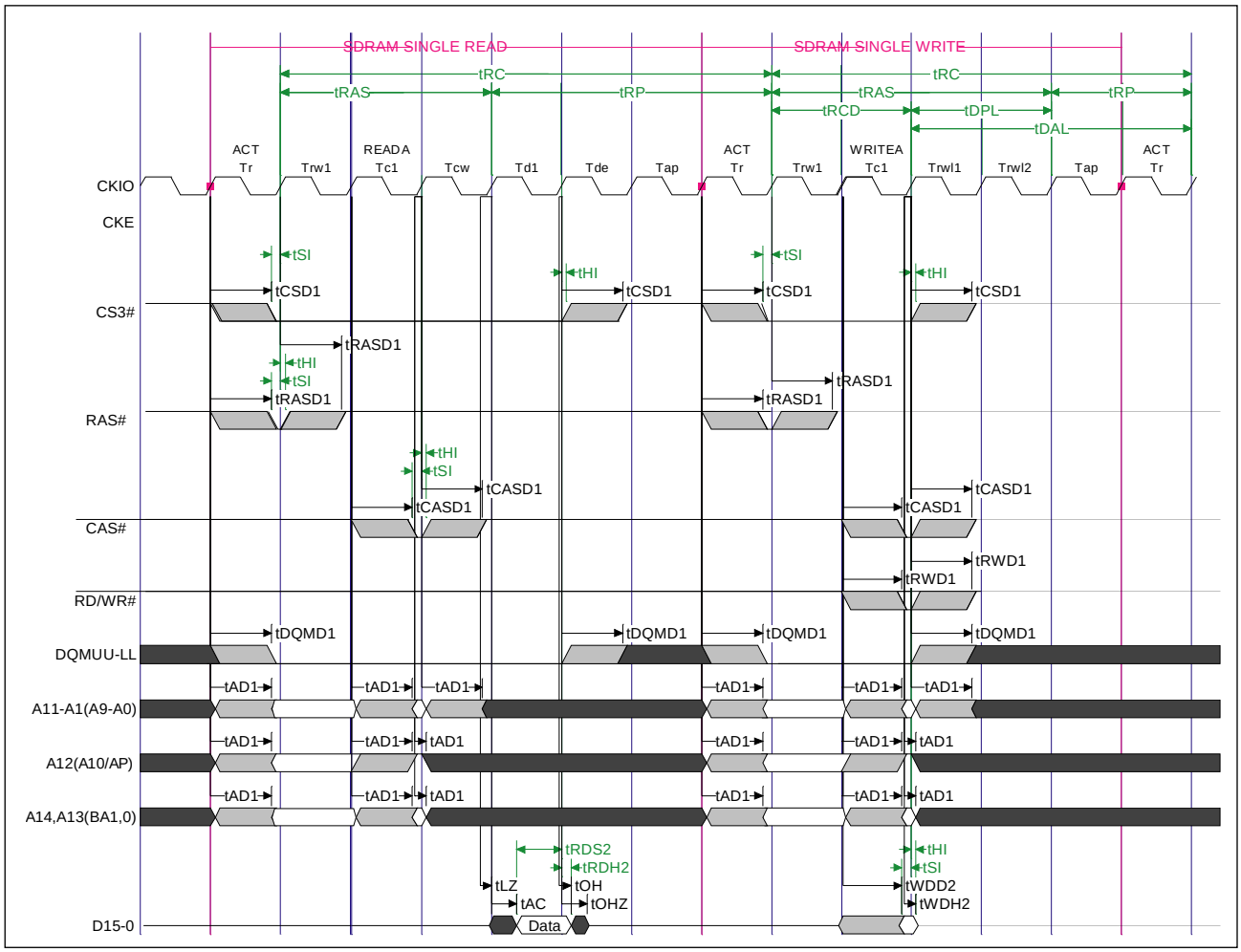

Figure 2.3.5 SDRAM Single Read/Write Timing

2.3.4 External EEPROM

The M3A-HS19 is provided with an EEPROM for storing MAC address.

Access to the EEPROM is enabled by using the SH7261 I/O ports (PC03, PC02, PC01 and PC00). A MAC address consists of 48-bit numbers.

Table 2.3.6 lists instruction sets, and Figure 2.3.6 shows the block diagram of CPU and EEPROM connection.

Figure 2.3.7 shows the EEPROM-AC timing and Figure 2.3.8 shows EEPROM-read/write timing.

Settings for following instruction sets are not required;

- A7 to A0 for WRAL, ERAL, EWEN, and EWDS instructions
- Data for ERASE, ERAL, EWEN and EWDS instructions

Table 2.3.6 Instruction Sets (S-93C76AFT)

Command	SK	Start Bit	Operation Code		Address			Data
		1	2	3	4	5	6~13	14~29
READ		1	1	0	-	A8	A7~A0	D15~D0 (OUT)
WRITE		1	0	1	-	A8	A7~A0	D15~D0 (IN)
ERASE		1	1	1	-	A8	A7~A0	-
WRAL		1	0	0	0	1	-	D15~D0(IN)
ERAL		1	0	0	1	0	-	-
EWEN		1	0	0	1	1	-	-
EWDS		1	0	0	0	0	-	-

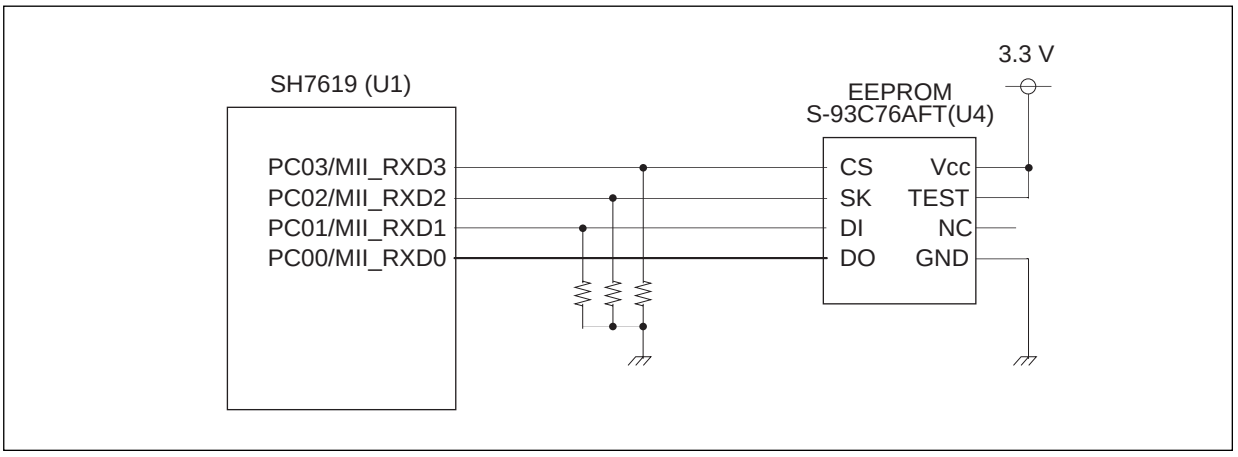

Figure 2.3.6 CPU and EEPROM Connection

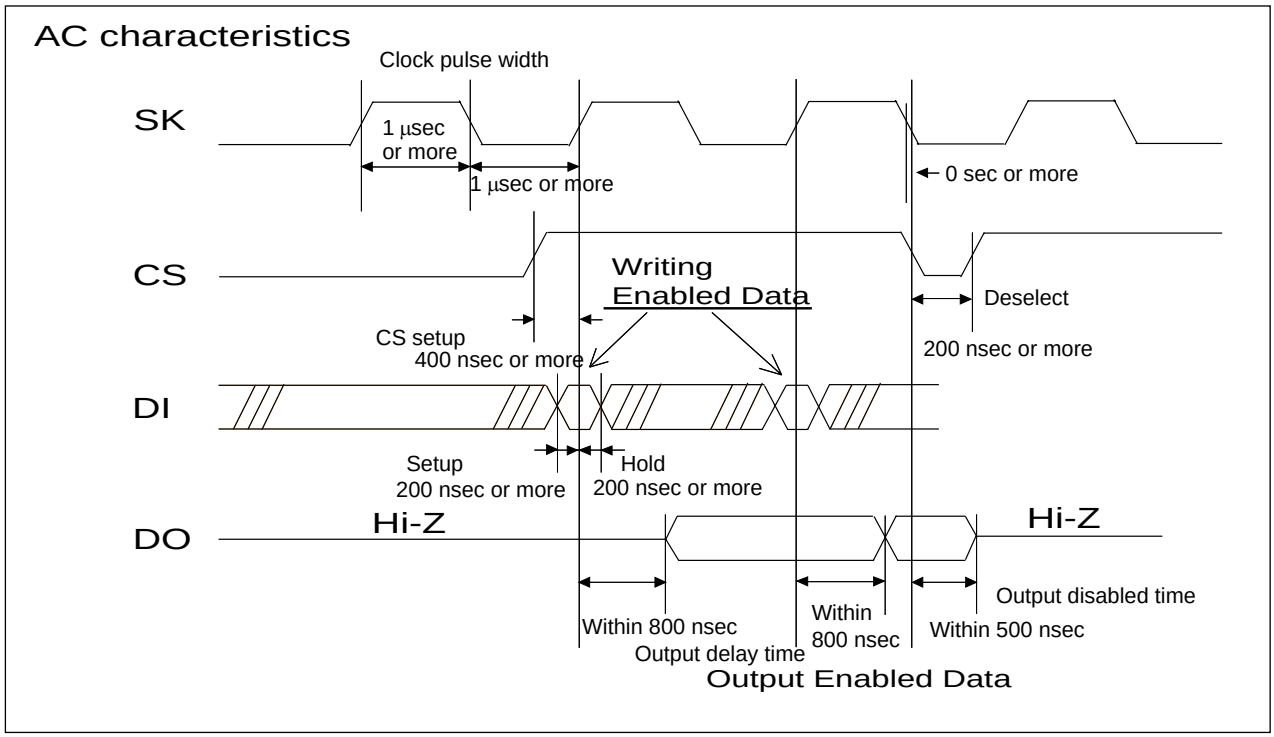

Figure 2.3.7 EEPROM-AC Timing

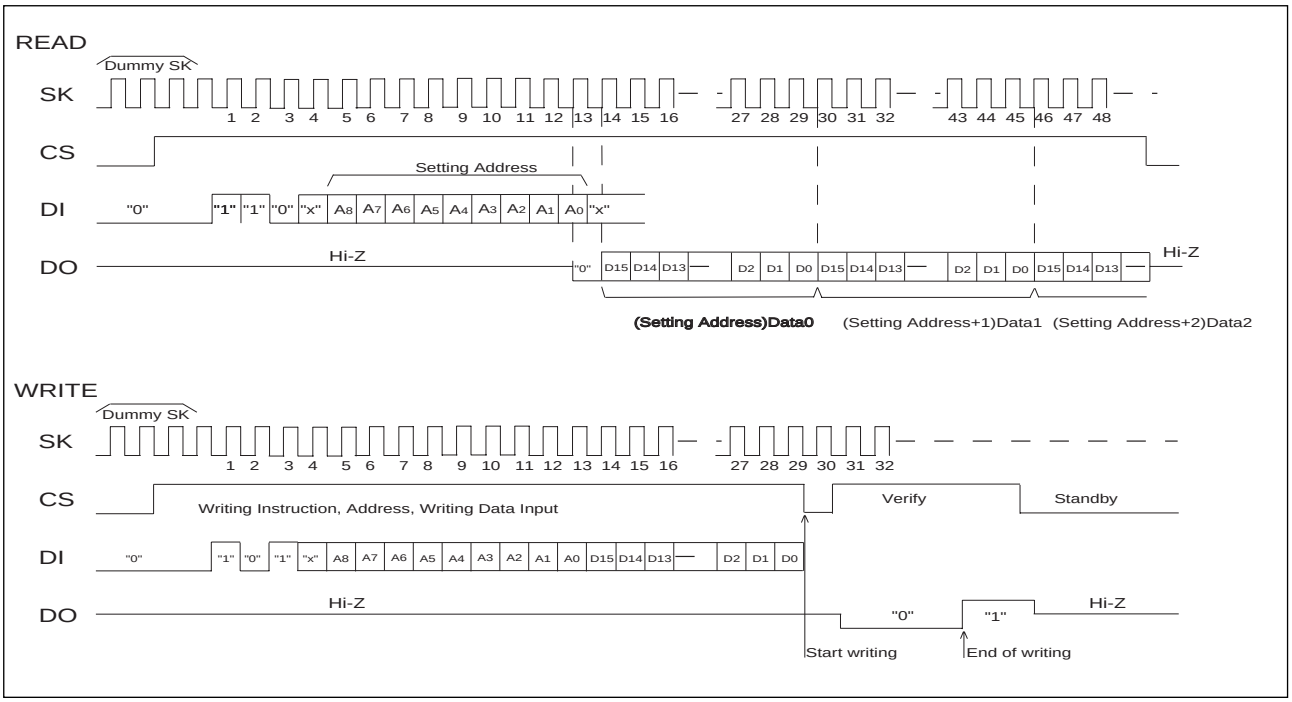

Figure 2.3.8 EEPROM-Read/Write Timing

2.4 Serial Port Interface

The SH7619 MCU mounted on the M3A-HS19 is provided with a 3 channel's of the Serial Communication Interface with FIFO (SCIF).

SCIF channel 0 is connected to the 2-pin serial port connector, SCIF channel 2 is connected to the D-sub 9-pin serial port connector, and SCIF channel 1 is connected to the 4-pin serial port connector.

Figure 2.4.1 shows the block diagram of the serial port interface.

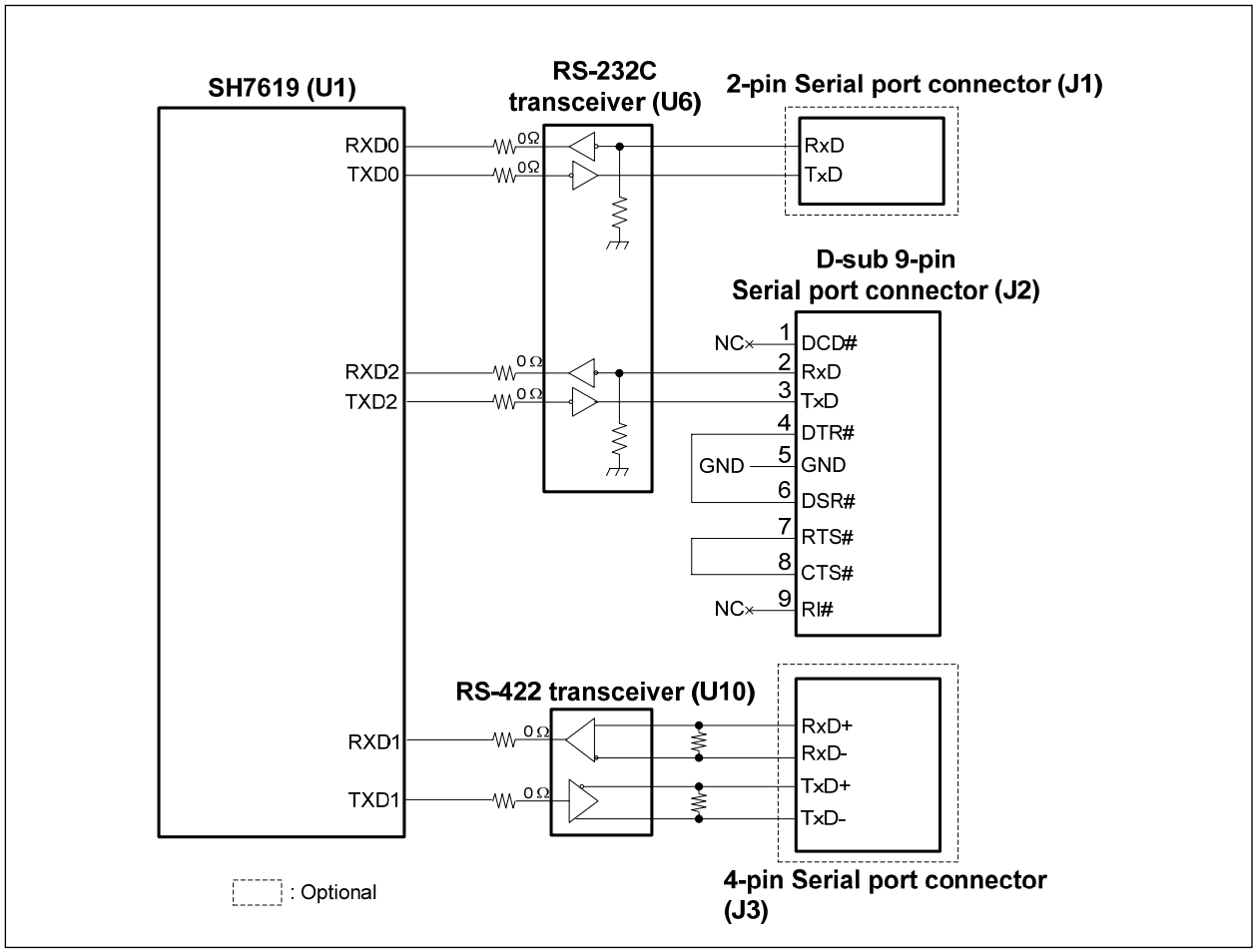

Figure 2.4.1 Serial Port Interface

2.5 PCMCIA Card Interface

The SH7619 MCU mounted on the M3A-HS19 is compliant with the JEIDA 4.2 (PCMCIA2.1 Rev.2.1). However, only 3.3 V interface PC card is supported. An on-chip bus state controller (BSC) and a PFC control the PC card.

High byte and low byte of the data is switched at the bus switch on the M3A-HS19. When the byte order of the SH7619 is big-endian, the order of the PC card connector is little-endian (IOIS16#: "L").

The M3A-HS19 is provided with a PCMCIA card slot in area 5, allowing both IC memory card and I/O card to be mounted.

Figure 2.5.1 shows the block diagram of PCMCIA card interface.

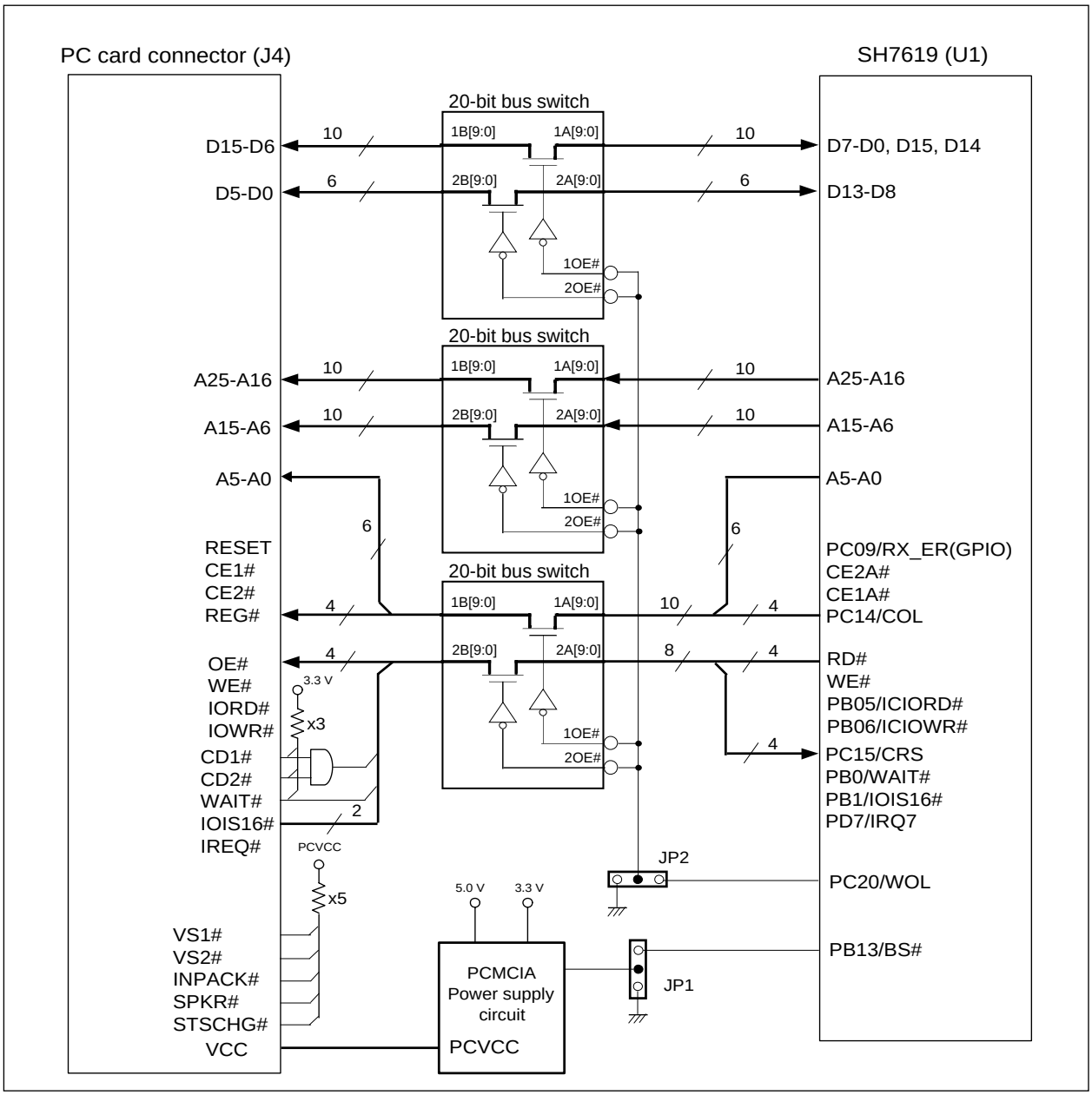

Figure 2.5.1 PCMCIA Card Interface

2.6 LAN Port Interface

An IEEE 802.3 compliant (MAC layer) Ethernet controller and an IEEE802.3/802.3u compliant (10/100 Mbps Ethernet PHY) physical layer transceiver are embedded in the SH7619 MCU.

Figure 2.6.1 shows the block diagram of LAN port interface.

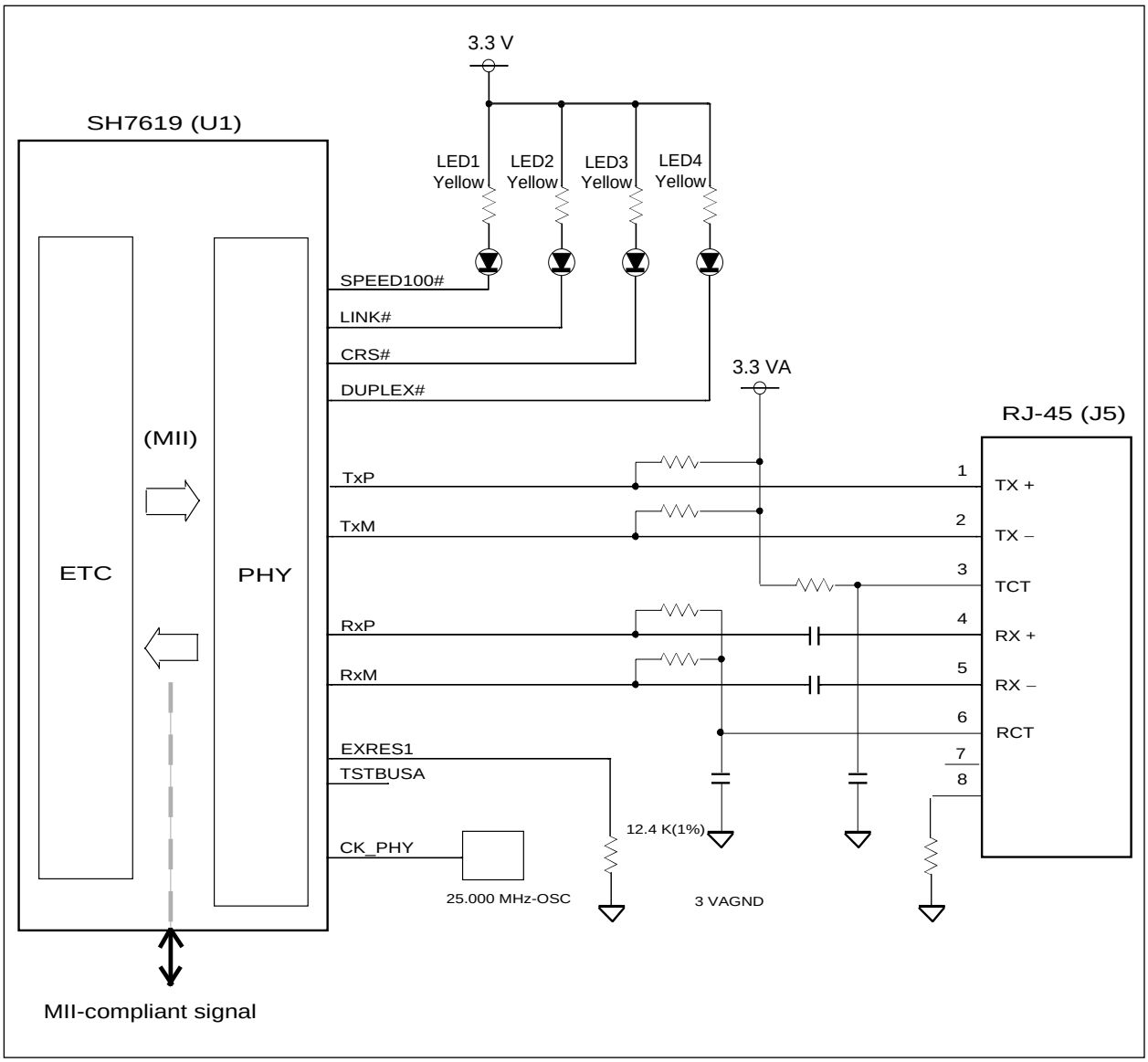

Figure 2.6.1 LAN Port Interface

2.7 I/O Port

Following I/O ports on the M3A-HS19 can be configured by the SH7619 MCU. These ports are multiplexed pins with up to four features. Some pins have several initial features for normal mode and HIF (Host Interface) boot mode. Features can be controlled by PFC (pin function controller).

- PA16 - PA25
- PB00 - PB13
- PC00 - PC20
- PD0 - PD7
- PE00 - PE24

The M3A-HS19 is connected with a memory, expansion connectors, a PCMCIA connector, a LAN connector, an RS-232C connector, an RS-422 connector and other control ICs. Some I/O ports are connected to DIP switches and LEDs, which can be used in the port mode as intended use. LED shows status in the PHY mode.

Table 2.7.1 lists Mode DIP Switch (SW4) Features. The state will be loaded when the board is reset and started.

Table 2.7.1 Mode DIP Switch (SW4) Features

SW4-No.	Description	
1	ON: Big-endian	OFF: Little-endian
2	ON: Host interface (HIF) is NOT operating	OFF: Host interface (HIF) is operating
3	ON: Normal boot mode	OFF: HIF boot mode
4	ON: Flash ROM is write-protected	OFF: Write-enabled

Figure 2.7.1 shows the block diagram of I/O port connections to switches and LEDs.

Table 2.7.2 and Table 2.7.3 list I/O port features.

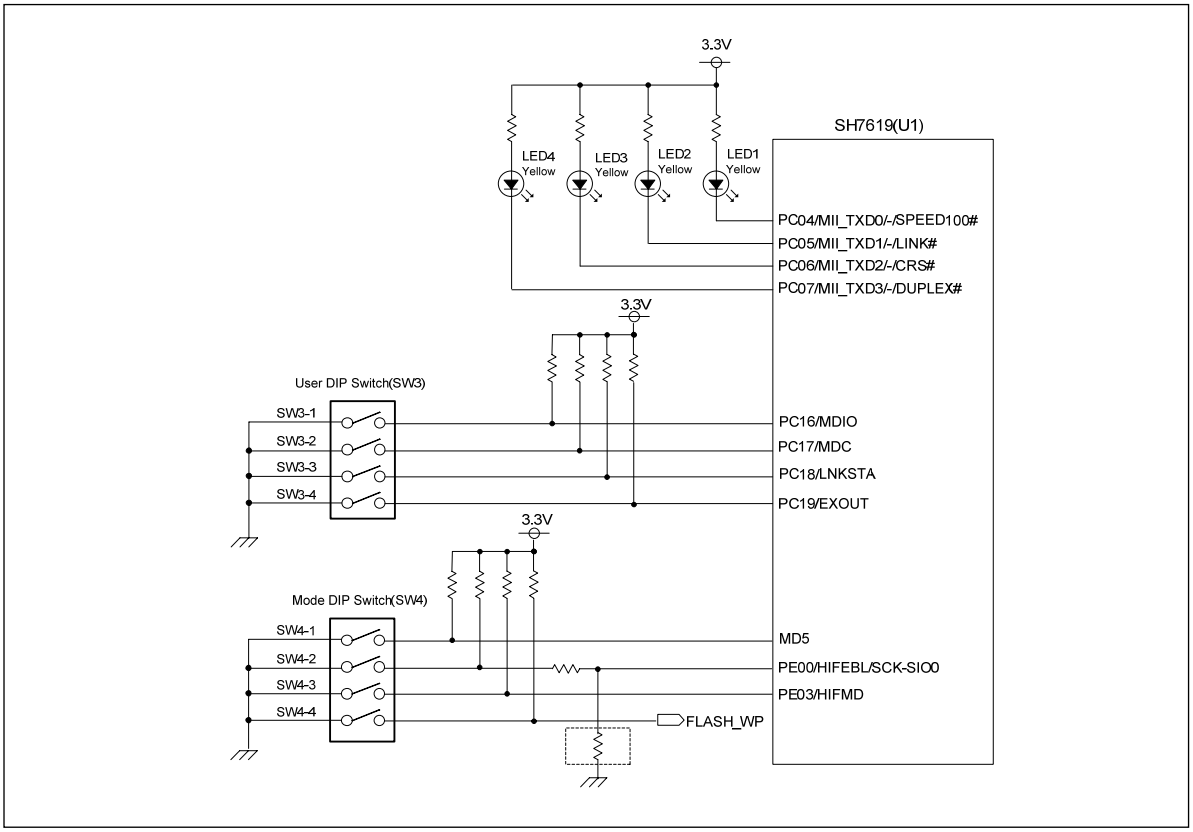

Figure 2.7.1 I/O Port Connection to Switches and LEDs

Table 2.7.2 I/O Port Features (1/2)

Port Name (SH7619)	Signal Name and Connection (M3A-HS19)
PA16~PA20	A16~A20: Flash ROM, PCMCIA, expansion connector
PA21	A21/SCK_SIO0: Flash ROM, PCMCIA, expansion connector
PA22	A22/SIOMCLK0: Flash ROM, PCMCIA, expansion connector
PA23	A23/RxD_SIO0: Flash ROM, PCMCIA, expansion connector
PA24	A24/TxD_SIO0: PCMCIA, expansion connector
PA25	A25/SIOFSYNC0: PCMCIA, expansion connector
PB0	WAIT#: PCMCIA
PB1	IOIS16#: PCMCIA
PB2	CKE: SDRAM
PB3	CAS#: SDRAM
PB4	RAS#: SDRAM
PB5	WE2#/DQMUL/ICIORD#: PCMCIA, expansion connector
PB6	WE3#/DQMUU/ICIOWR#: PCMCIA, expansion connector
PB7	CE2B#: Expansion connector
PB8	CS6B#/CE1B#: Expansion connector
PB9	CE2A#: PCMCIA
PB10	CS5B#/CE1A#: PCMCIA
PB11	CS4#: Expansion connector
PB12	CS3#: SDRAM, expansion connector
PB13	BS#: PCMCIA-PW control, expansion connector
PC0~PC3	MII_RxD0~MII_RxD3: EEPROM, expansion connector
PC4	MII_TxD0/SPEED100#: LED1
PC5	MII_TxD1/LINK#: LED2
PC6	MII_TxD2/CRS#: LED3
PC7	MII_TxD3/DUPLEX#: LED4
PC8	RX_DV: Expansion connector
PC9	RX_ER: PCMCIA
PC10	RX_CLK: Expansion connector
PC11	TX_ER: Expansion connector
PC12	TX_EN: Expansion connector
PC13	TX_CLK: Expansion connector
PC14	COL: PCMCIA
PC15	CRS: PCMCIA, expansion connector
PC16	MDIO: SW3-1 (Port IN)
PC17	MDC: SW3-2 (Port IN)
PC18	LNKSTA: SW3-3 (Port IN)
PC19	EXOUT: SW3-4 (Port IN)
PC20	WOL: PCMCIA (Bus DIR) , expansion connector
PD0	IRQ0/TEND0: SW6(IRQ0)
PD1	IRQ1/TEND1: Expansion connector

Table 2.7.3 I/O Port Features (2/2)

Port Name (SH7619)	Signal Name and Connection (M3A-HS19)
PD2	IRQ2/TxD1/DREQ0: RS-422
PD3	IRQ3/RxD1/DACK0: RS-422
PD4	IRQ4/SCK1: Expansion connector
PD5	IRQ5/TxD2/DREQ1: RS-232C
PD6	IRQ6/RxD2/DACK1: RS-232C
PD7	IRQ7/SCK2: PCMCIA, expansion connector
PE0	HIFEBL/SCK_SIO0: SW4-2, expansion connector
PE1	HIFRDY/SIOMCLK0: Expansion connector
PE2	HIFDREQ/RxD_SIO0: Expansion connector
PE3	HIFMD: SW4-3
PE4	HIFINT#/TxD_SIO0: Expansion connector
PE5	HIFRD#: Expansion connector
PE6	HIFWR#/SIOFSYNC: Expansion connector
PE7	HIFRS: Expansion connector
PE8	HIFCS#: Expansion connector
PE9~PE14	HIFD0~HIFD5/D16~D21: Expansion connector
PE15	HIFD6/TxD0/D22: Expansion connector, 3-wire RS-232C
PE16	HIFD7/RxD0/D23: Expansion connector, 3-wire RS-232C
PE17	HIFD8/SCK0/D24: Expansion connector
PE18	HIFD9/TxD1/D25: Expansion connector
PE19	HIFD10/RxD1/D26: Expansion connector
PE20	HIFD11/SCK1/D27: Expansion connector
PE21	HIFD12/RTS0/D28: Expansion connector
PE22	HIFD13/CTS0/D29: Expansion connector
PE23	HIFD14/RTS1/D30: Expansion connector
PE24	HIFD15/CTS1/D31: Expansion connector

2.8 Power Supply Circuit

The main power supply input 5 V DC to the M3A-HS19 and it generates 3.3 V and 1.8 V using a regulator.
It is an adjustable output voltage regulator to generate a desired voltage by changing resistance values.
A through-hole is provided with the M3A-HS19 to input 1.8 V DC from an external power supply. The PC card power supply is controlled by software.
Figure 2.8.1 shows the schematic diagram of the power supply circuit.

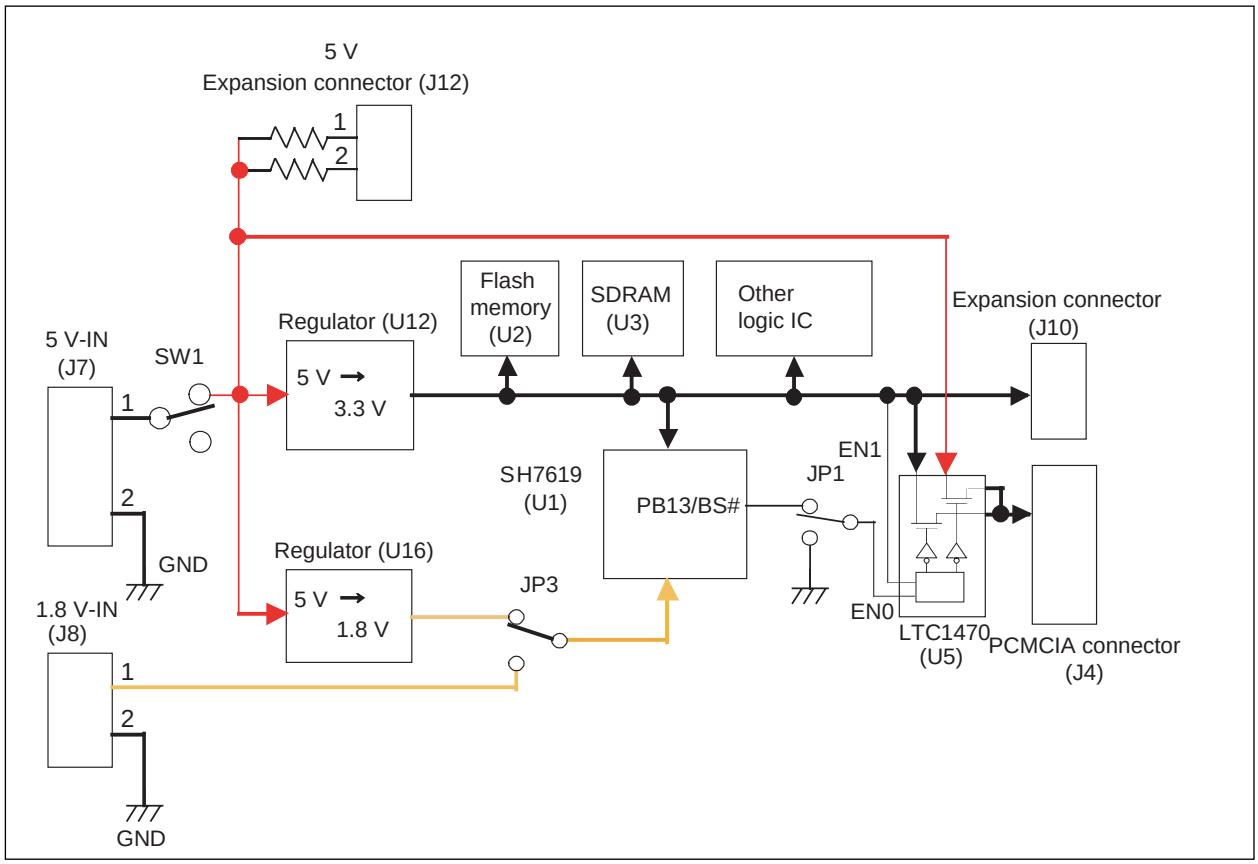

Figure 2.8.1 Power Supply Circuit

2.9 Clock Module

The clock module on the M3A-HS19 consists of following three blocks;

- A block connecting X1 (oscillator) output to SH7619 EXTAL
- A block connecting X2 (ceramic resonator) to EXTAL and XTAL (Optional)
- A block connecting X3 (oscillator) to CK-PHY

An on-chip oscillator (15.625 MHz) is connected to the SH7619 MCU to provide an operating clock. Another on-chip oscillator (25.000 MHz) is also connected to the MCU to provide clock to physical layer. Bus clock output is connected to a SDRAM and expansion connectors via damping resisters respectively.

Figure 2.9.1 shows the block diagram of clock module.

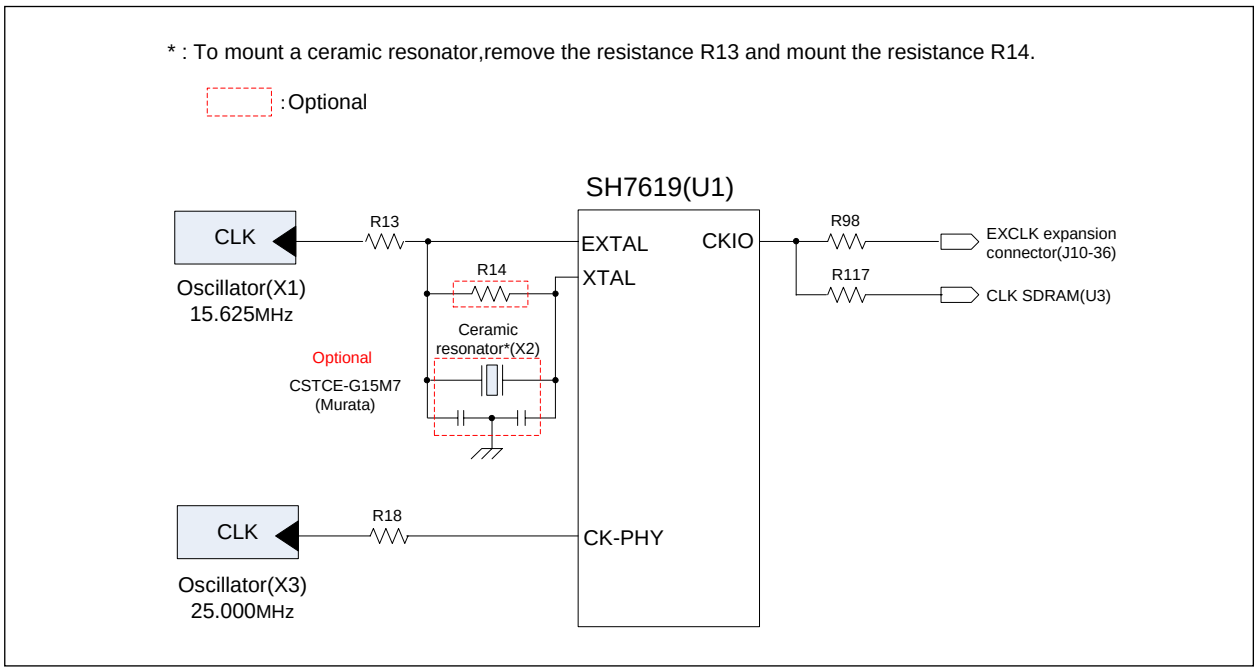

Figure 2.9.1 Clock Module

2.10 Reset Module

Reset module controls reset signals connected to the SH7619 MCU, a flash memory and connectors. Software controls to reset PCMCIA connector.

Figure 2.10.1 shows the schematic diagram of resets.

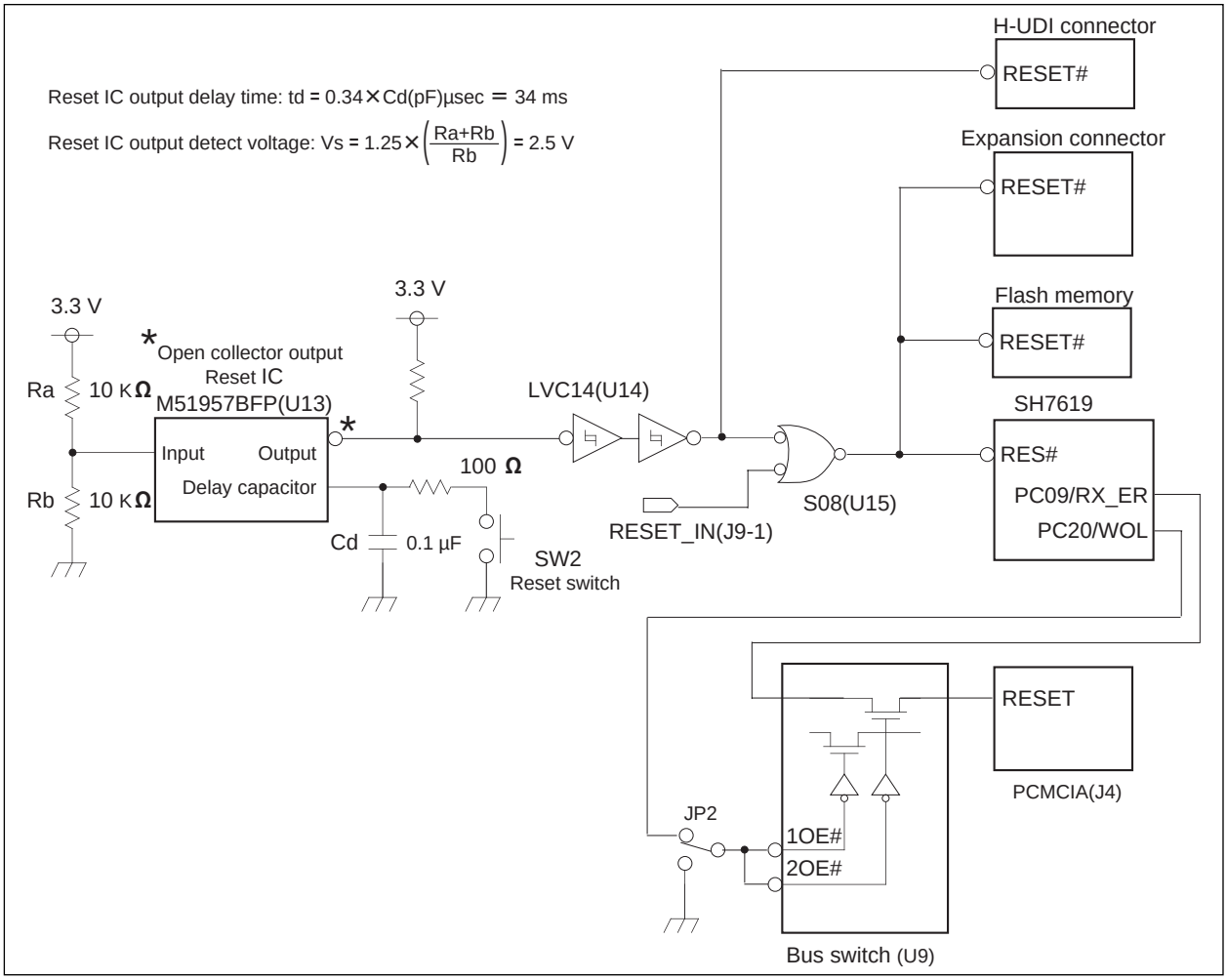

Figure 2.10.1 M3A-HS19 Reset System

2.11 Interrupt Switch

Push-button switches are connected to the SH7619 NMI pin and IRQ0 pin.

Interrupts are connected to IRQ7 from an expansion connector and a PCMCIA connector.

Figure 2.11.1 shows the schematic diagram of interrupts.

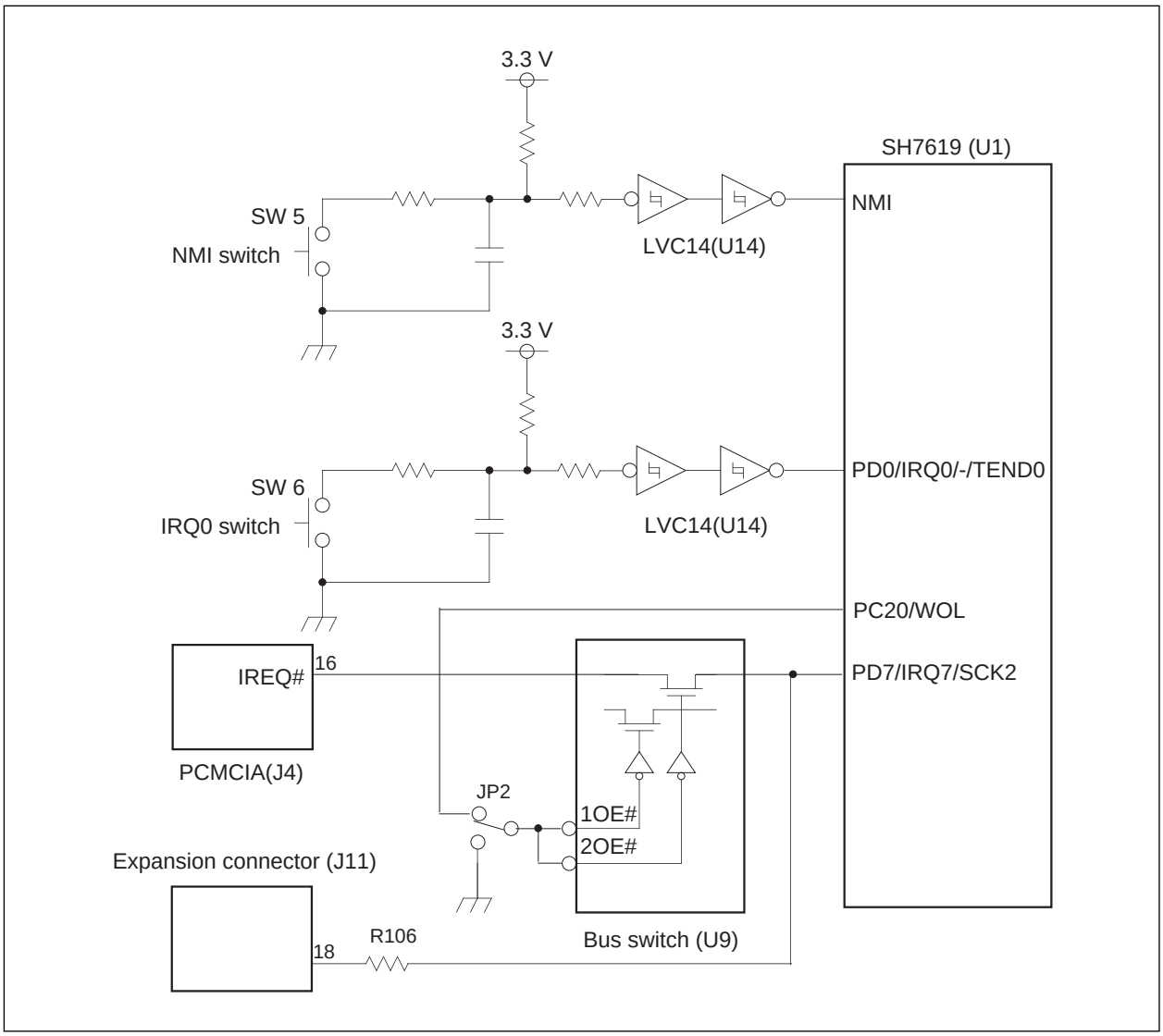

Figure 2.11.1 Interrupts

2.12 E10A-USB Interface

The M3A-HS19 is provided with a 14-pin H-UDI connector to embed the E10A-USB emulator.

Figure 2.12.1 shows the block diagram of the E10A-USB interface.

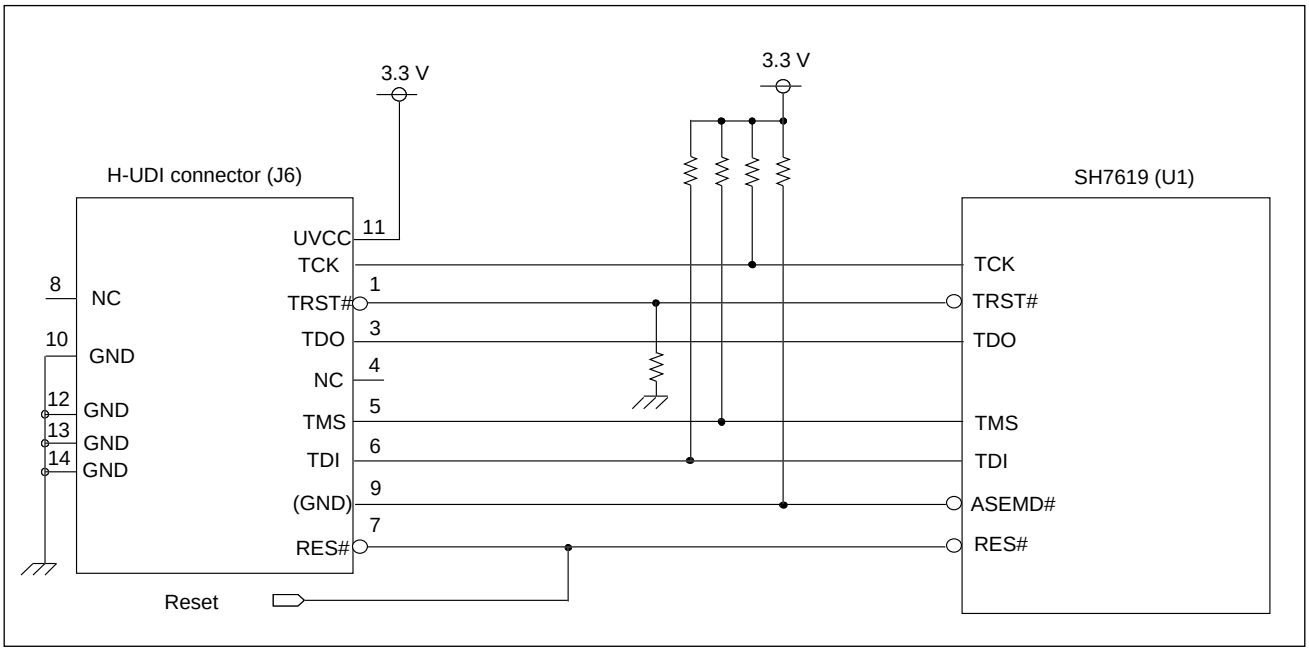

Figure 2.12.1 E10A-USB Interface

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Chapter3
Operational Specifications

3.1 M3A-HS19 Connectors

Figure 3.1.1 shows the connector assignments on the M3A-HS19.

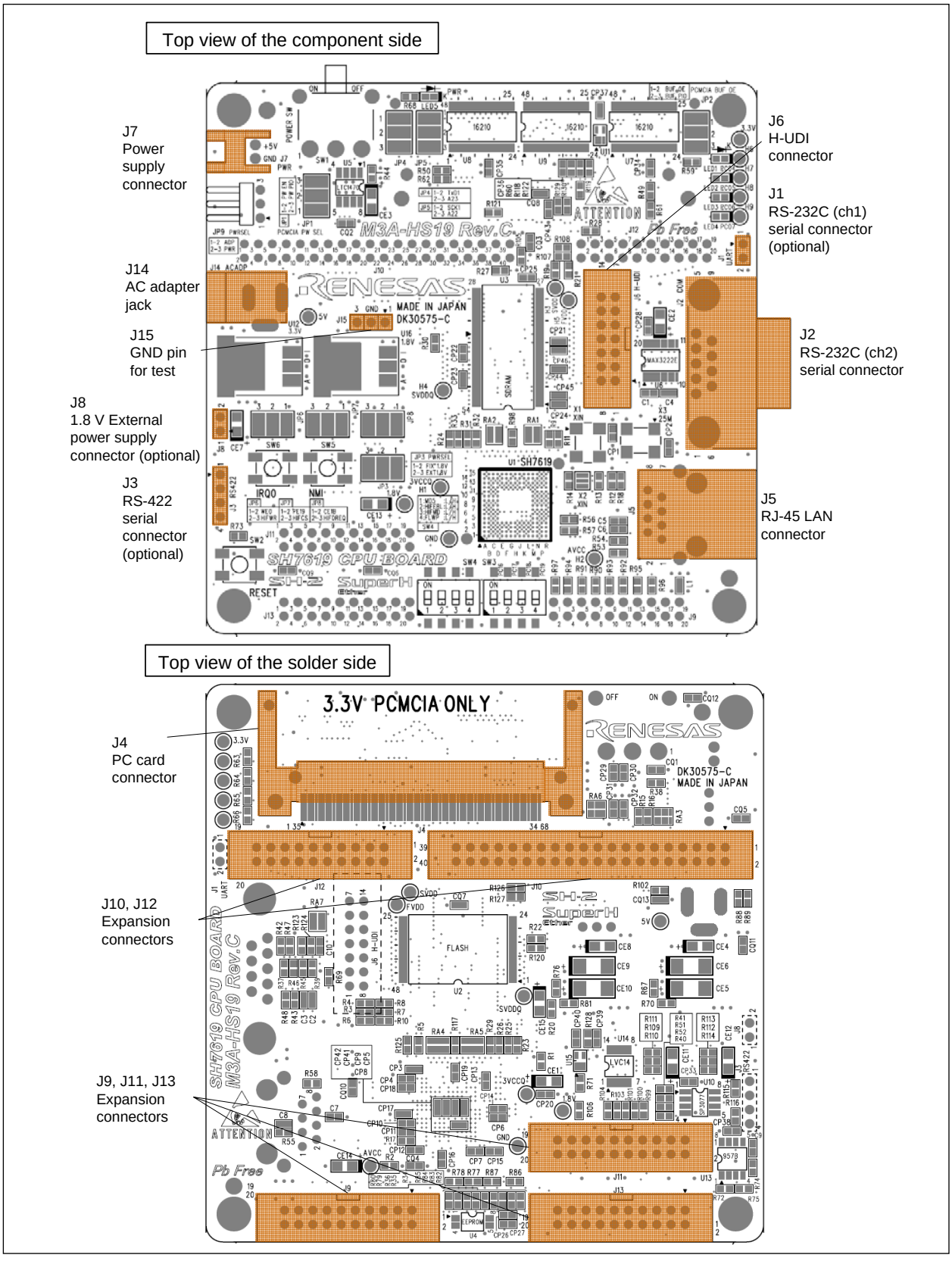


Figure 3.1.1 M3A-HS19 Connector Assignments

3.1.1 UART Connector Pin (J1)

The M3A-HS19 is provided with an UART connector pin (J1).

Figure 3.1.2 shows the pin assignment for the UART connector (J1).

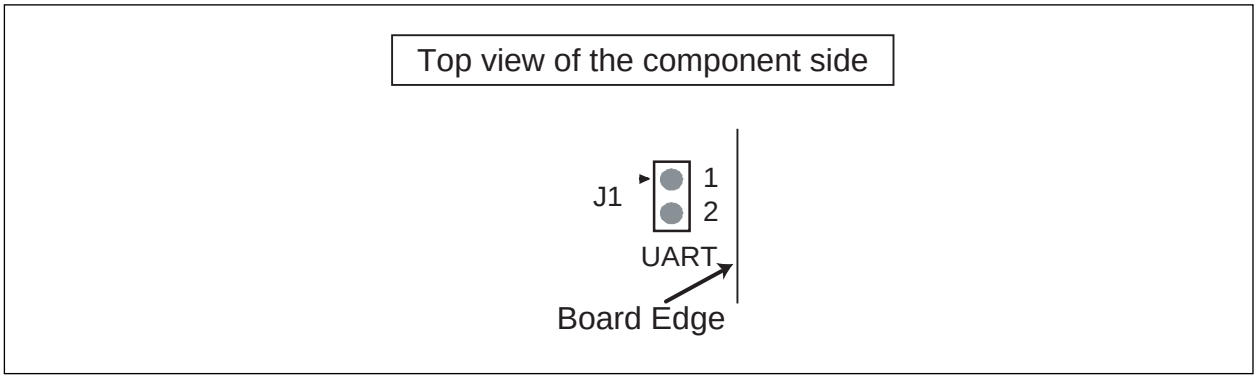


Figure 3.1.2 Pin assignment for UART Connector (J1)

Table 3.1.1 lists the pin assignment for the UART connector (J1).

Table 3.1.1 Pin assignment for UART Connector (J1)

Pin no.	Signal Name	Pin no.	Signal Name
1	RXD (PE16/HIFD07/RXD0/D23)	2	TXD (PE15/HIFD06/TXD0/D22)

3.1.2 UART Connector (J2)

The M3A-HS19 is provided with an UART connector (J2).

Figure 3.1.3 shows the pin assignment for the UART connector (J2).

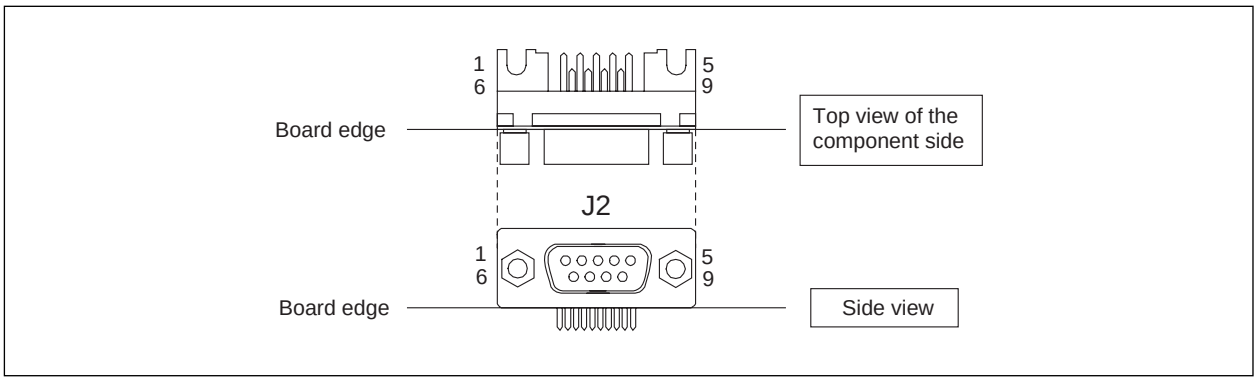


Figure 3.1.3 Pin assignment for UART Connector (J2)

Table 3.1.2 lists the pin assignment for the UART connector (J2).

Table 3.1.2 Pin assignment for UART Connector (J2)

Pin no.	Signal Name	Pin no.	Signal Name
1	NC	6	DSR#
2	RXD (PD6/IRQ6/RXD2/DACK1)	7	RTS#
3	TXD (PD5/IRQ5/TXD2/DREQ1)	8	CTS#
4	DTR#	9	NC
5	GND		

Pins 4-6 and 7-8 are loopback-connected, respectively.

3.1.3 RS-422 Connector Pin (J3)

The M3A-HS19 is provided with an RS-422 connector pin (J3).

Figure 3.1.4 shows the pin assignment for the RS-422 connector pin (J3).

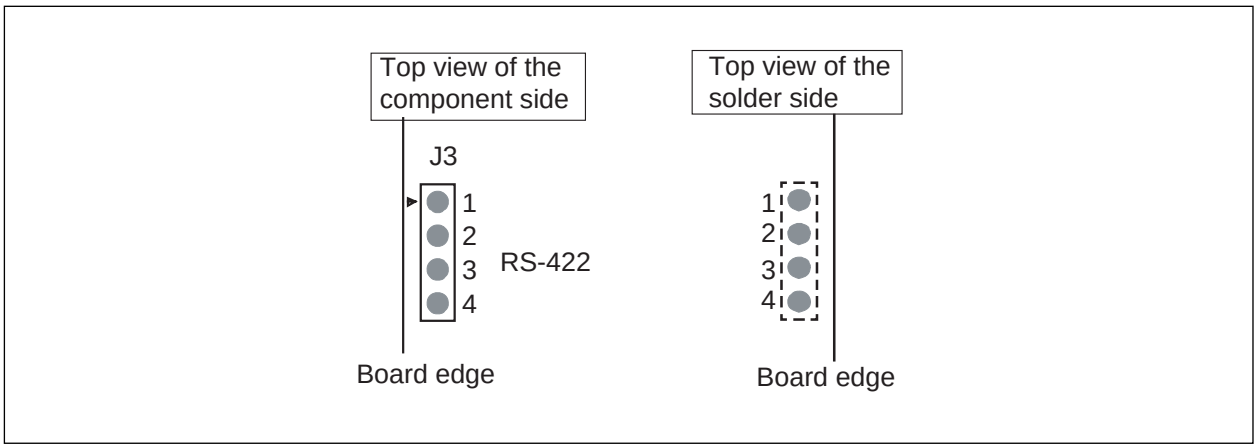


Figure 3.1.4 Pin assignment for RS-422 Connector Pin (J3)

Table 3.1.3 lists the pin assignment for the RS-422 connector pin (J3).

Table 3.1.3 Pin assignment for RS-422 Connector Pin (J3)

Pin no.	Signal Name	Pin no.	Signal Name
1	RXD-a (PD3/IRQ3/RXD1/DACK0)	3	TXD-z (PD2/IRQ23/TXD1/DREQ0)
2	RXD-b (PD3/IRQ3/RXD1/DACK0)	4	TXD-y (PD2/IRQ23/TXD1/DREQ0)

3.1.4 PCMCIA Connector (J4)

The M3A-HS19 is provided with a PCMCIA connector (J4).

Figure 3.1.5 shows the pin assignment for the PCMCIA connector (J4).

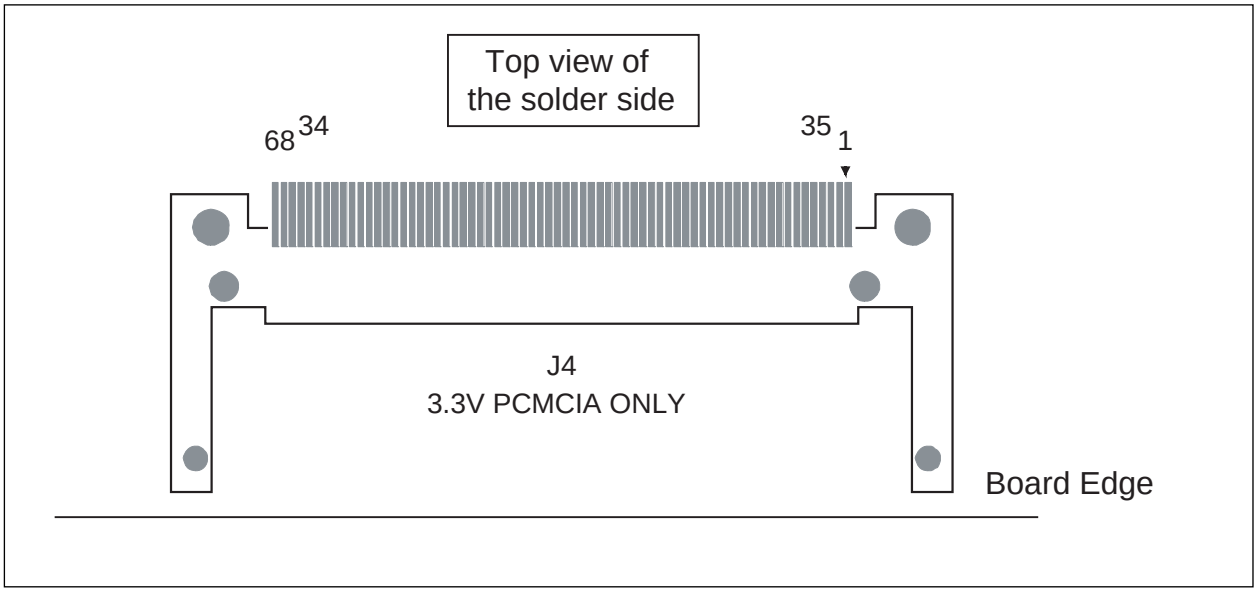


Figure 3.1.5 Pin assignment for PCMCIA Connector (J4)

Table 3.1.4 lists the pin assignment for the PCMCIA connector (J4).

Table 3.1.4 Pin assignment for PCMCIA Connector (J4)

Pin no.	Signal Name	Pin no.	Signal Name
1	GND	35	GND
2	D3	36	CD1# (PC15/CRS)
3	D4	37	D11
4	D5	38	D12
5	D6	39	D13
6	D7	40	D14
7	CE1# (CE2A#)	41	D15
8	A10	42	CE2# (CE1A#)
9	OE# (RD#)	43	VS1# (Pulled up to the PCMCIA power supply)
10	A11	44	IORD# (PB05/WE2#/DQMUL/ICIORD#)
11	A9	45	IOWR# (PB06/WE3#/DQMUU/ICIOWR#)
12	A8	46	A17
13	A13	47	A18
14	A14	48	A19
15	WE# (WE1#/DQMLU/WE#)	49	A20
16	IREQ# (PD7/IRQ7/SCK2)	50	A21
17	VCC	51	VCC
18	VPP1	52	VPP2
19	A16	53	A22
20	A15	54	A23
21	A12	55	A24
22	A7	56	A25
23	A6	57	VS2# (Pulled up to the PCMCIA power supply)
24	A5	58	RESET (PC09/RX_ER)
25	A4	59	WAIT# (PB00/WAIT#)
26	A3	60	INPACK# (Pulled up to the PCMCIA power supply)
27	A2	61	REG# (PC14/COL)
28	A1	62	SPKR# (Pulled up to the PCMCIA power supply)
29	A0	63	STSCHG# (Pulled up to the PCMCIA power supply)
30	D0	64	D8
31	D1	65	D9
32	D2	66	D10
33	IOIS16# (PB01/IOIS16#)	67	CD2# (PC15/CRS)
34	GND	68	GND

3.1.5 LAN Connector (J5)

The M3A-HS19 is provided with a LAN connector (J5).

Figure 3.1.6 shows the pin assignment for the LAN connector (J5).

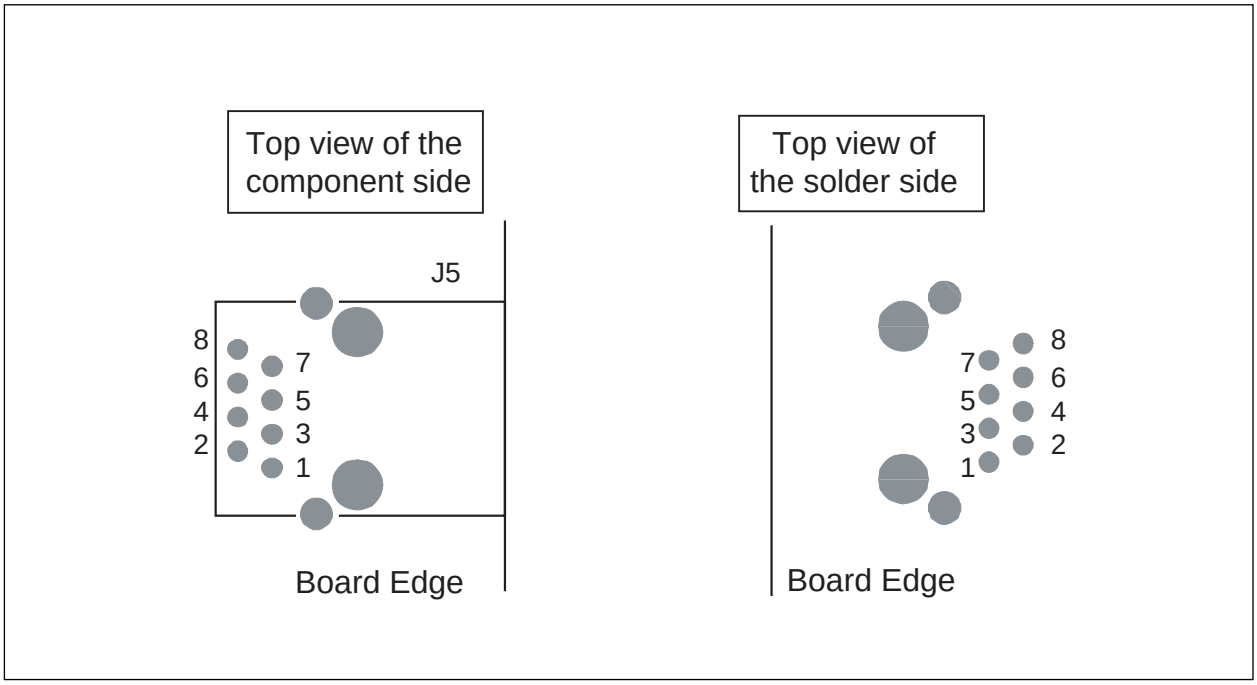


Figure 3.1.6 Pin assignment for LAN Connector (J5)

Table 3.1.5 lists the pin assignment for the LAN connector (J5).

Table 3.1.5 Pin assignment for LAN Connector (J5)

Pin no.	Signal Name	Pin no.	Signal Name
1	TD+	5	RD-
2	TD-	6	RCT
3	TCT	7	NC
4	RD+	8	NC

3.1.6 H-UDI Connector (J6)

The M3A-HS19 is provided with an H-UDI (J6) connector to connect the E10A-USB emulator.
Figure 3.1.7 shows the pin assignment for the H-UDI connector (J6).

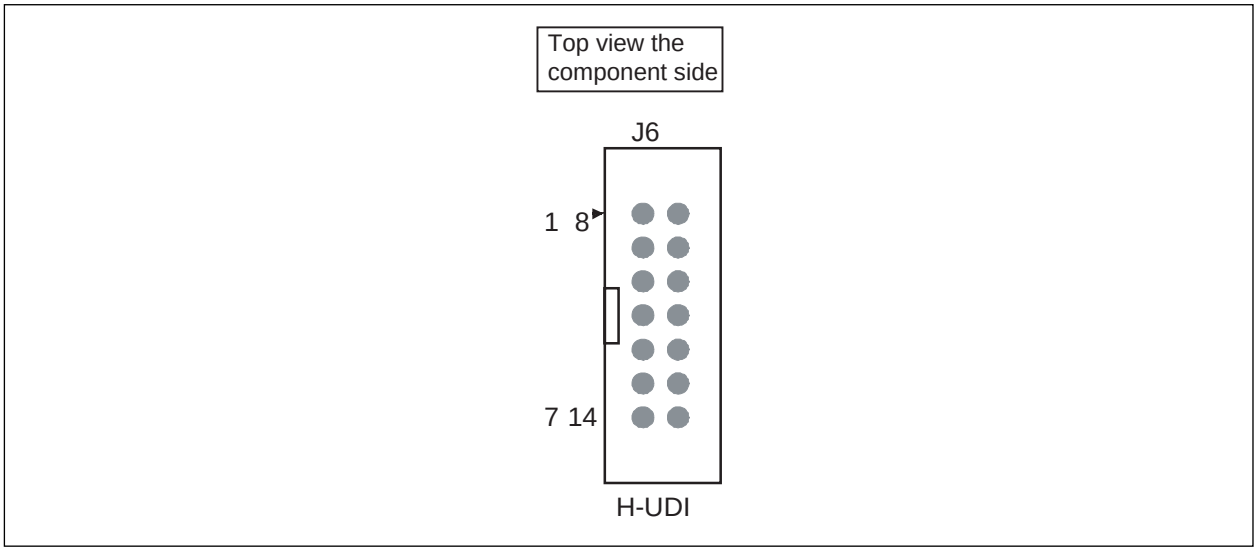


Figure 3.1.7 Pin assignment for H-UDI Connector (J6)

Table 3.1.6 lists the pin assignment for the H-UDI connector (J6).

Table 3.1.6 Pin assignment for H-UDI Connector (J6)

Pin no.	Signal Name	Pin no.	Signal Name
1	TCK	8	N.C.
2	TRST#	9	(GND) ASEMD#
3	TDO	10	GND
4	N.C.	11	UVCC
5	TMS	12	GND
6	TDI	13	GND
7	RESET#	14	GND

3.1.7 Power Supply Connector (J7)

The M3A-HS19 is provided with a connector for power supply.

Figure 3.1.8 shows the pin assignment for the power supply connector (J7).

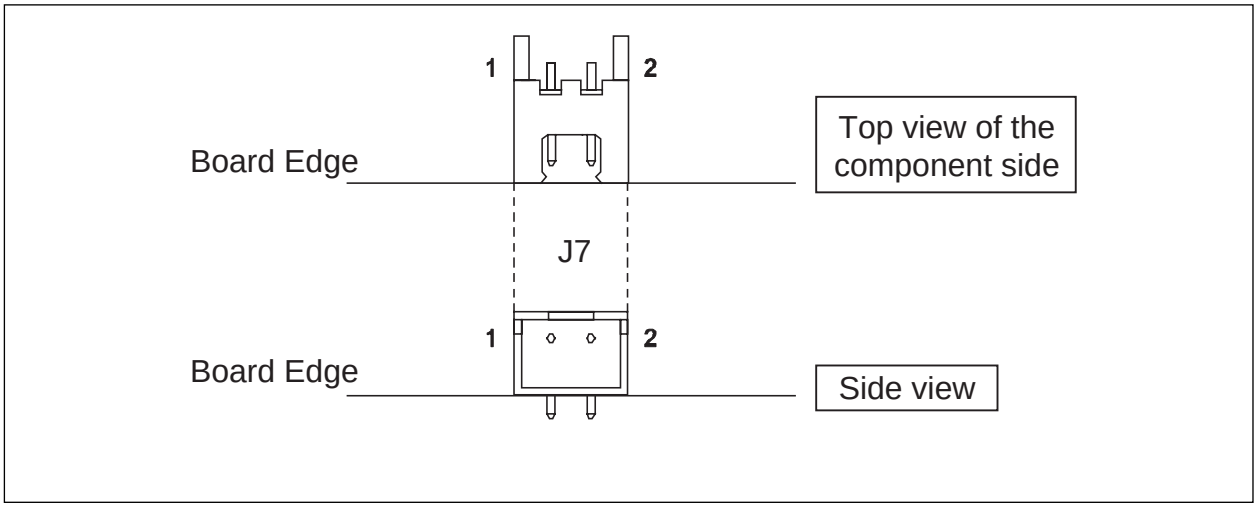


Figure 3.1.8 Pin assignment for Power Supply Connector (J7)

Table 3.1.7 lists the pin assignment for the power supply connector (J7).

Table 3.1.7 Pin assignment for Power Supply Connector (J7)

Pin no.	Signal Name	Pin no.	Signal Name
1	+5 V	2	GND

3.1.8 External Power Supply Connector (J8)

The M3A-HS19 is provided with a through-hole for the SH7619 external power supply connector (J8: Supplies 1.8 V). Figure 3.1.9 shows the pin assignment for the external power supply connector (J8).

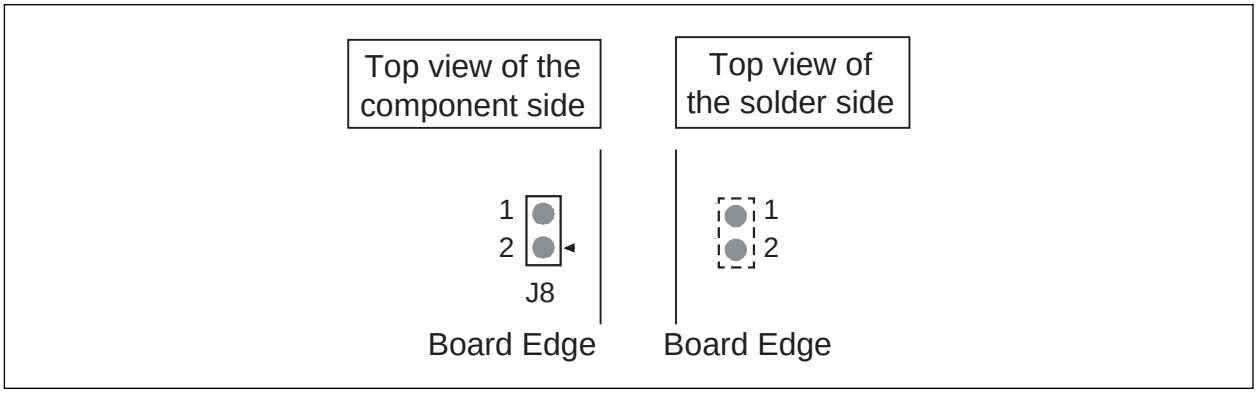


Figure 3.1.9 Pin assignment for External Power Supply Connector (J8)

Table 3.1.8 lists the pin assignment for the external power supply connector (J8).

Table 3.1.8 Pin assignment for External Power Supply Connector (J8)

Pin no.	Signal Name	Pin no.	Signal Name
1	+1.8 V	2	GND

3.1.9 Expansion Connectors (J9-J13)

The M3A-HS19 is provided with through-holes for expansion connectors. The Through-holes are connected to the SH7619 I/O pins. Expansion connectors (J9 - J13) can be connected to the MIL STD connector to mount expansion boards or to monitor the SH7619 bus signals.

Figure 3.1.10 shows the pin assignment for expansion connectors.

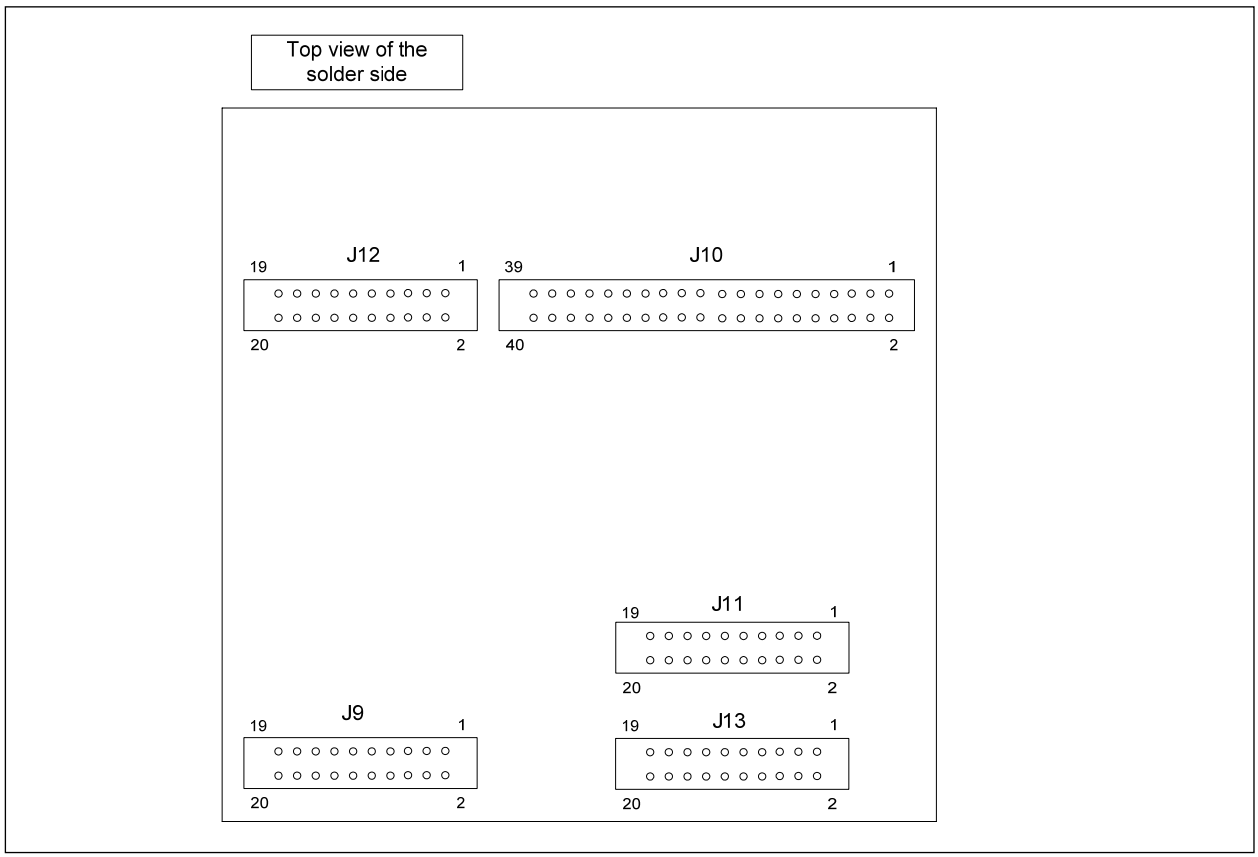


Figure 3.1.10 Pin assignment for Expansion Connectors

Table 3.1.9 lists the pin assignment for the expansion connector (J9).

Table 3.1.9 Pin assignment for Expansion Connector (J9)

Pin no.	Signal Name	Pin no.	Signal Name
1	RESET_IN#	2	PB00/WAIT#
3	PB13/BS#	4	PA25/SIOFSYNC0
5	PC01/MII_RXD1	6	PD3/IRQ3/RXD1/DACK0
7	PC00/MII_RXD0	8	PD2/IRQ2/TXD1/DREQ0
9	PC03/MII_RXD3	10	PE07/HIFRS
11	PC02/MII_RXD2	12	PE01/HIFRDY
13	PC20/WOL	14	NC
15	PC15/CRS	16	PE04/HIFINT#
17	NC	18	NC
19	GND	20	GND

Table 3.1.10 Pin assignment for Expansion Connector (J10)

Pin no.	Signal Name	Pin no.	Signal Name
1	+3.3 V	2	+3.3 V
3	GND	4	GND
5	NC	6	PA23/A23/RXD_SIO0, PE18/HIFD09/TxD1/D25 Jumper select
7	PA22/A22/SIOMCLK0, PD4/IRQ4/SCK1 Jumper select	8	PA22/A22/SIOMCLK0
9	PA21/A21/SCK_SIO0	10	PA20/A20
11	PA19/A19	12	PA18/A18
13	PA17/A17	14	PA16/A16
15	A15	16	A14
17	A13	18	A12
19	A11	20	A10
21	A9	22	A8
23	A7	24	A6
25	A5	26	A4
27	A3	28	A2
29	A1	30	A0
31	PC13/TX_CLK	32	PB07/CE2B#
33	PC12/TX_EN	34	GND
35	PB11/CS4#	36	CKIO
37	PC08/RX_DV	38	CS0#
39	RES#	40	GND

Table 3.1.11 Pin assignment for Expansion Connector (J13)

Pin no.	Signal Name	Pin no.	Signal Name
1	PE24/HIFD15/CTS1/D31	2	PE23/HIFD14/RTS1/D30
3	PE22/HIFD13/CTS0/D29	4	PE21/HIFD12/RTS0/D28
5	PE20/HIFD11/SCK1/D27	6	PE19/HIFD10/RXD1/D26
7	PE18/HIFD09/TXD1/D25	8	PE17/HIFD08/SCK0/D24
9	PE16/HIFD07/RXD0/D23	10	PE15/HIFD06/TXD0/D22
11	PE14/HIFD05/-/D21	12	PE13/HIFD04/-/D20
13	PE12/HIFD03/-/D19	14	PE11/HIFD02/-/D18
15	PE10/HIFD01/-/D17	16	PE09/HIFD00/-/D16
17	PE06/HIFWR#/SIOFSYNC0	18	PE08/HIFCS#
19	PE05/HIFRD#	20	GND

Table 3.1.12 Pin assignment for Expansion Connector (J12)

Pin no.	Signal Name	Pin no.	Signal Name
1	+5 V	2	+5 V
3	RD#	4	DD15
5	DD14	6	DD13
7	DD12	8	DD11
9	DD10	10	DD9
11	DD8	12	DD7
13	DD6	14	DD5
15	DD4	16	DD3
17	DD2	18	DD1
19	DD0	20	GND

Table 3.1.13 Pin assignment for Expansion Connector (J11)

Pin no.	Signal Name	Pin no.	Signal Name
1	PD0/IRQ0/-/TEND0	2	PD1/IRQ1/-/TEND1
3	PB12/CS3#	4	RD/WR#
5	WE0#/DQMLL , PE06/HIFWR#/SIOFSYNC0 Jumper select	6	WE1#/DQMLU/WE# (connected by on-chip resistor) Optional
7	PB05/WE2#(BE2)/DQMUL/ICIORD#	8	PB06/WE3#(BE3)/DQMUU/ICIOWR#
9	NC	10	NC
11	NC	12	PE19/HIFD10/RxD1/D26 ,PE08/HIFCS# (Jumper select)
13	NC	14	PA24/A24/TXD_SIO0
15	PE00/HIFEBL/SCK_SIO0	16	PB08/CS6B#/CE1B#, PE02/HIFDREQ/RXD_SIO0 (Jumper select)
17	PC11/TX_ER	18	PD7/IRQ7/SCK2
19	PC10/RX_CLK	20	GND

3.2 Switches and LEDs

The M3A-HS19 is provided with switches and LEDs as its operational components. Figure 3.2.1 shows the assignment of operational components.

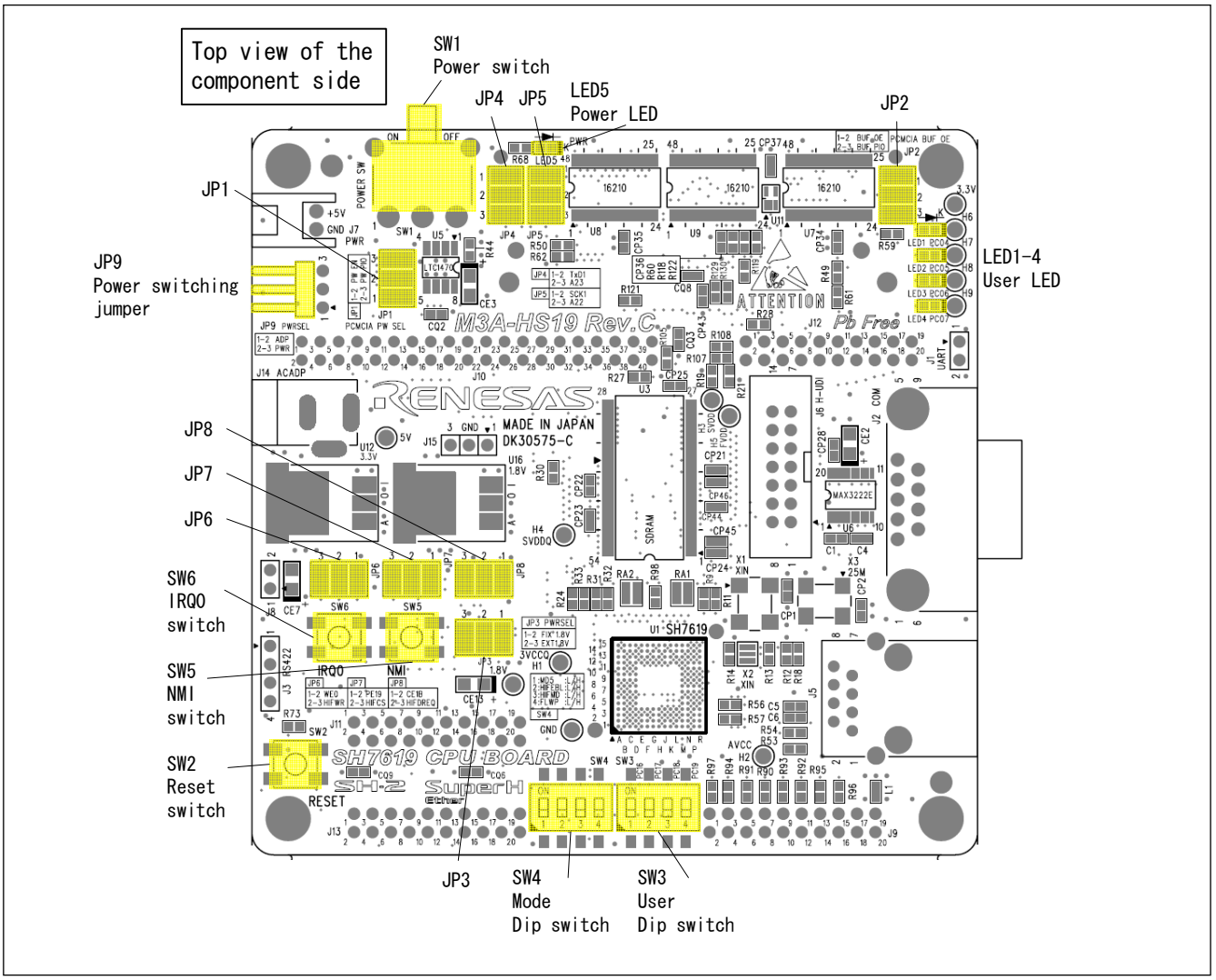


Figure 3.2.1 M3A-HS19 Operational Components Assignment

3.2.1 Jumpers (JP1 - JP9)

The M3A-HS19 is provided with nine jumpers.

Figure 3.2.2 shows the jumper assignments (JP1 - JP9), and Table 3.2.1 through Table 3.2.6 list the jumper settings (JP1 - JP9).

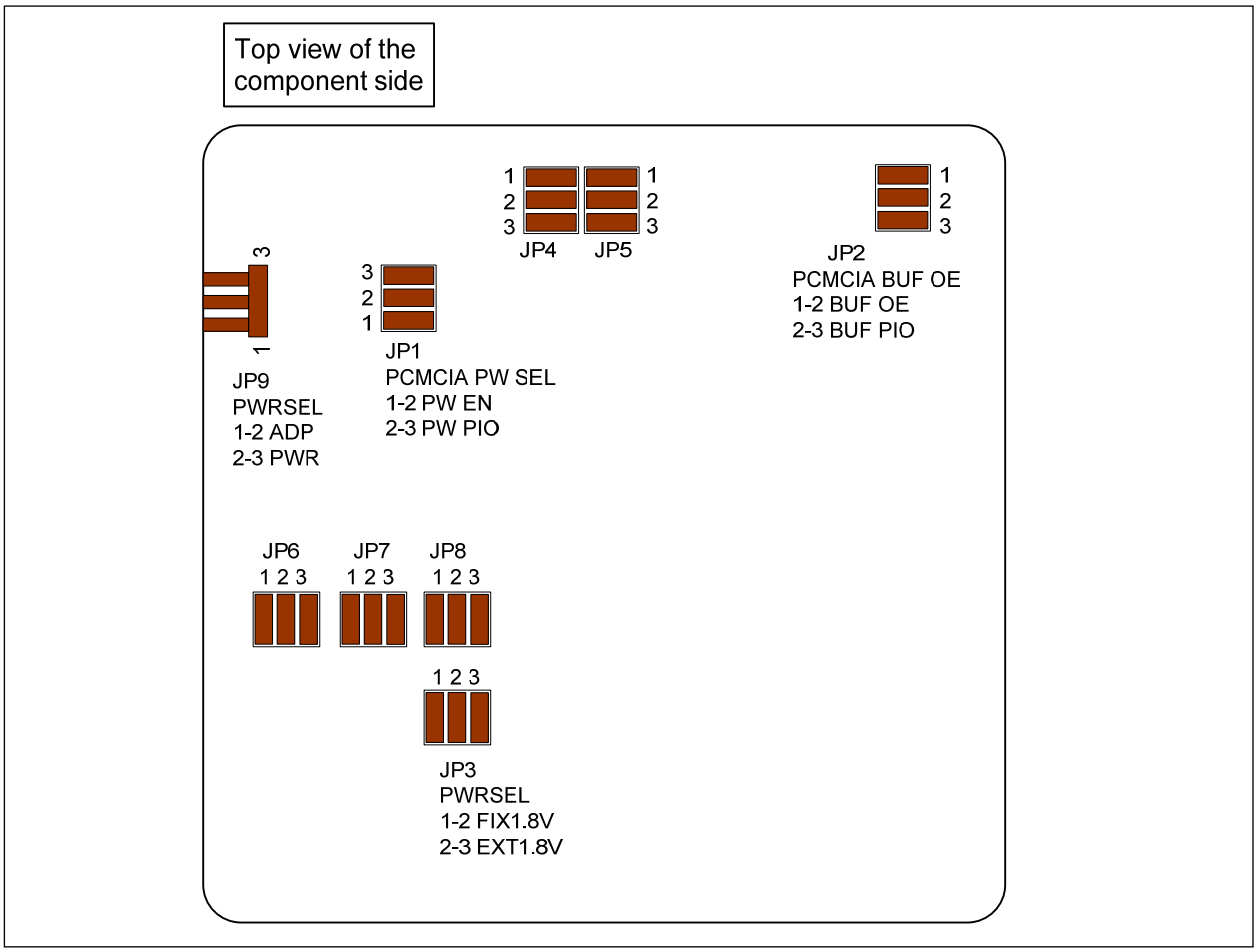


Figure 3.2.2 M3A-HS19 Jumpers Assignments (JP1 - JP9)

Table 3.2.1 M3A-HS19 Jumper Settings (JP1)

Jumper no.	Setting	Description
JP1 PCMCIAPWSEL	1-2	PW EN
	2-3	PW PIO

Table 3.2.2 M3A-HS19 Jumper Settings (JP2)

Jumper no.	Setting	Description
JP2 PCMCIABUFOE	1-2	BUF OE
	2-3	BUF PIO

Table 3.2.3 M3A-HS19 Jumper Settings (JP3)

Jumper no.	Setting	Description
JP3 PWRSEL	1-2	1.8 V-fixed power supply voltage (supplied from regulator)
	2-3	External power supply voltage (supplied from J8)

Table 3.2.4 M3A-HS19 Jumper Settings (JP4, JP5)

Jumper no.	Setting	Description
JP4	1-2	TxD1
	2-3	A23
JP5	1-2	SCK1
	2-3	A22

Table 3.2.5 M3A-HS19 Jumper Settings (JP6 - JP8)

Jumper no.	Setting	Description
JP6	1-2	WE0
	2-3	HIFWR
JP7	1-2	PE19
	2-3	HIFCS
JP8	1-2	CE1B
	2-3	HIFDREQ

Table 3.2.6 M3A-HS19 Jumper Settings (JP9)

Jumper no.	Setting	Description
JP9	1-2	AC adapter
	2-3	Power supply connector

indicates the default setting.

Note: Do not make any change with the jumper settings while the M3A-HS19 is operating. Ensure to turn the power OFF before changing the settings.

3.2.2 Features of Switches and LEDs

The M3A-HS19 is provided with six switches and five LEDs. Figure 3.2.3 shows the pin assignment for switches and LEDs. Table 3.2.7 lists the switches mounted on the M3A-HS19.

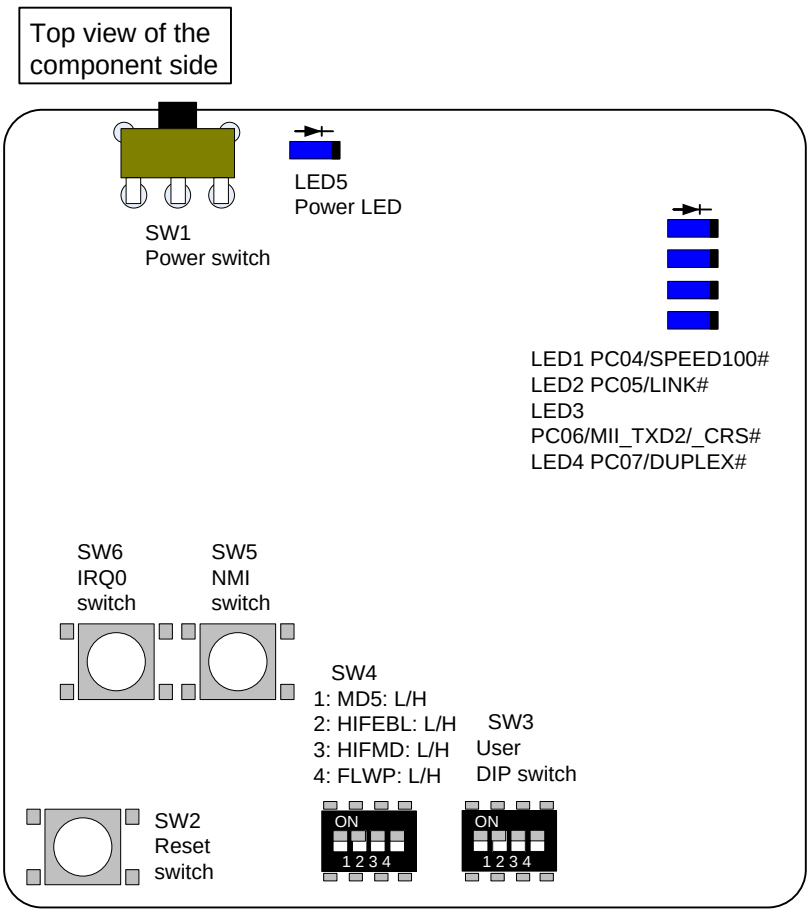


Figure 3.2.3 Pin assignment for Switches and LEDs

Table 3.2.7 Switches on the M3A-HS19

No.	Description	Remarks
SW1	System power on/off switch	-
SW2	System reset input switch	See section 2.10 for details.
SW3	User DIP switches (4/package) SW3-1 OFF: PC16 = "H" ON: PC16 = "L" SW3-2 OFF: PC17 = "H" ON: PC17 = "L" SW3-3 OFF: PC18 = "H" ON: PC18 = "L" SW3-4 OFF: PC19 = "H" ON: PC19 = "L"	PC16, PC17, PC18, and PC19 are pulled up. See section 2.7 for details.
SW4	Mode DIP switches (4/package)	See Table 3.2.8 for features.
SW5	NMI interrupt switch	See section 2.11 for details.
SW6	IRQ0 switch	See section 2.11 for details.

Table 3.2.8 lists the SW4 features. Indicates the default setting.

Table 3.2.8 SW4 Features

No.	Setting	Description		
SW4-1 MD5	OFF	MD5 = "H"	Little endian	Data alignment setting
	ON	MD5 = "L"	Big endian	
SW4-2 HIFEBL	OFF	HIFEBL = "H"	HIF pin is activated	
	ON	HIFEBL = "L"	HIF pin is released to activate	
SW4-3 HIFMD	OFF	HIFMD = "H"	Starts up from the host interface (HIF)	
	ON	HIFMD = "L"	Not start up from the host interface (HIF)	
SW4-4 FLASH_WP#	OFF	FLASH_WP# = "H"	Flash memory is write-enabled	
	ON	FLASH_WP# = "L"	Flash memory is write-protected	

Table 3.2.9 lists the LEDs on the M3A-HS19.

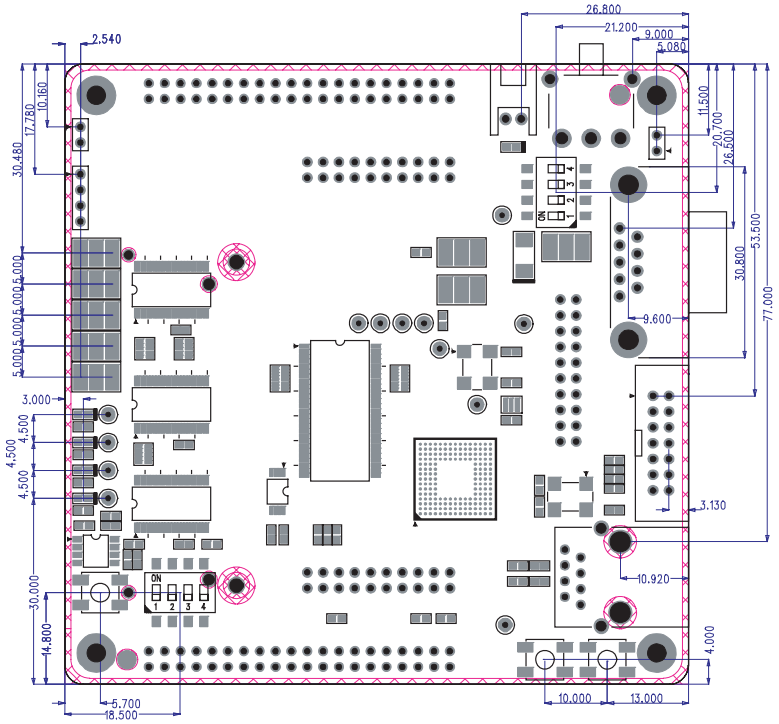
Table 3.2.9 LEDs

No.	Color	Description
LED1	Yellow	User LED (LED1 lights when PC04/SPEED100# outputs "L")
LED2	Yellow	User LED (LED2 lights when PC05/LINK# outputs "L")
LED3	Yellow	User LED (LED3 lights when PC06/MII_TXD2/-/CRS# outputs "L")
LED4	Yellow	User LED (LED4 lights when PC07/DUPLEX# outputs "L")
LED5	Blue	Power LED (LED5 lights when 3.3 V power is supplied)

3.3 Dimensions

Figure 3.3.1 shows the M3A-HS19 dimensions. Connectors can be mounted on J9 through J13 to simplify to mount an expansion board.

<Top view of the component side>



<Transparent view of the component side>

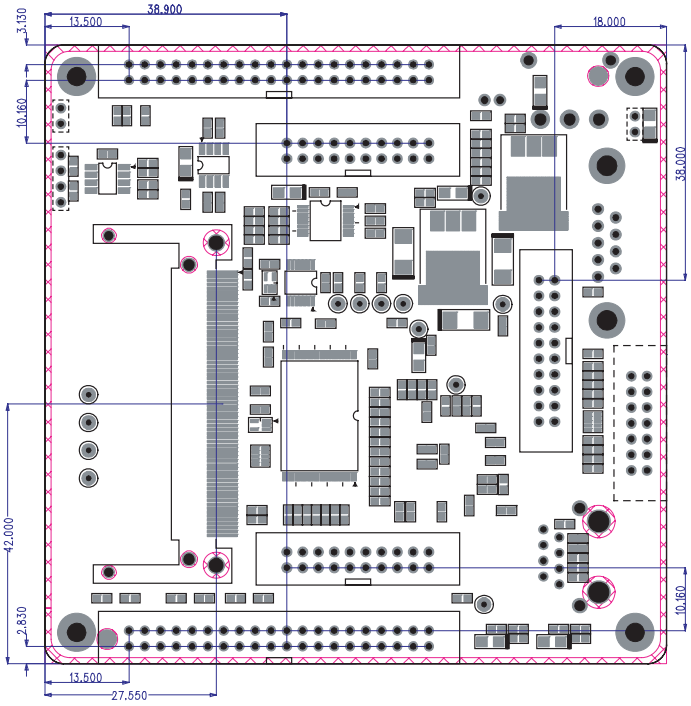


Figure 3.3.1 M3A-HS19 Dimensions

Appendix

M3A-HS19 SCHEMATICS

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SH-2 SH7619 CPU BOARD M3A-HS19 Rev.C SCHEMATICS

Note:
VCC = 5V
3VCC = 3.3V
1.8VCC = 1.8V

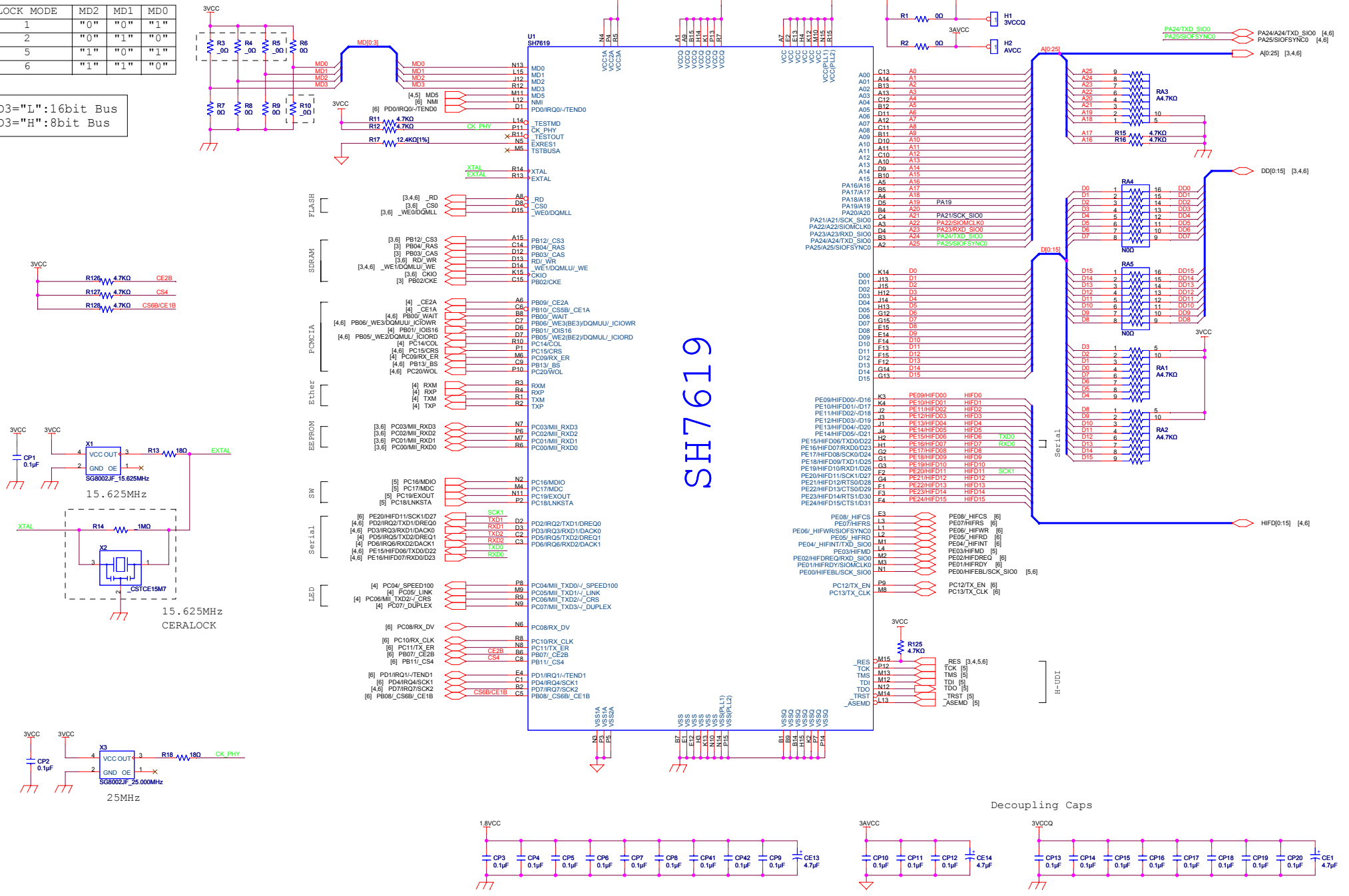
R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

[Note] [----] :not mounted

CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS19
		SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 7)
Ver.1.01		DATE 08-08-19					DK30575-C

CLOCK MODE	MD2	MD1	MD0
1	"0"	"0"	"1"
2	"0"	"1"	"0"
5	"1"	"0"	"1"
6	"1"	"1"	"0"

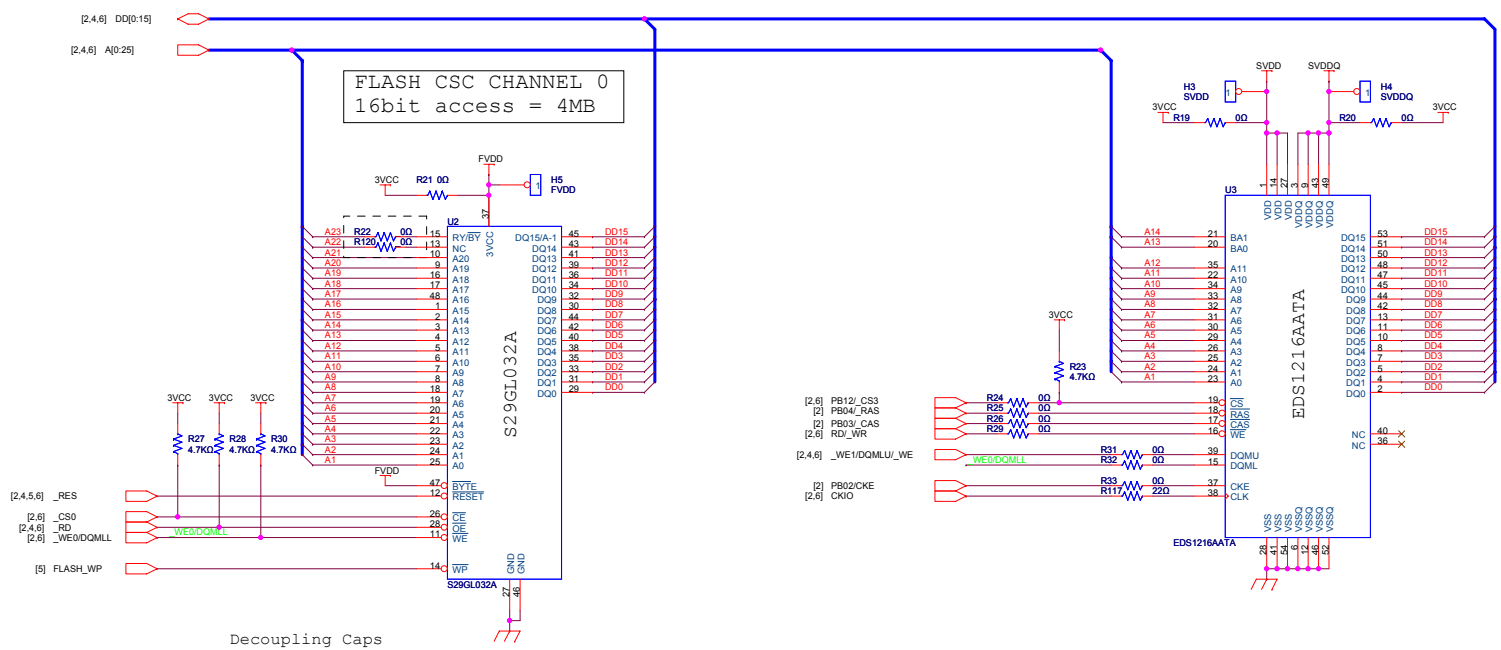
MD3="L":16bit Bus
MD3="H":8bit Bus



CHANGE			RENESAS SOLUTIONS CORPORATION	M3A-HS19
Ver.1.01	SCALE		DRAWN / CHECKED / DESIGNED / APPROVED	CPU SH7619 (2 / 7)
	DATE	08-08-19		DK30575-C

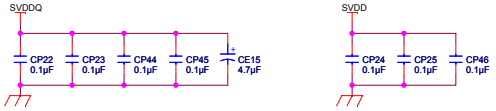
FLASH MEMORY

SDRAM

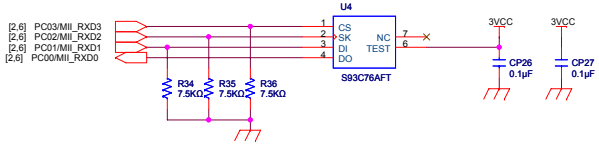


Decoupling Caps

Decoupling Caps

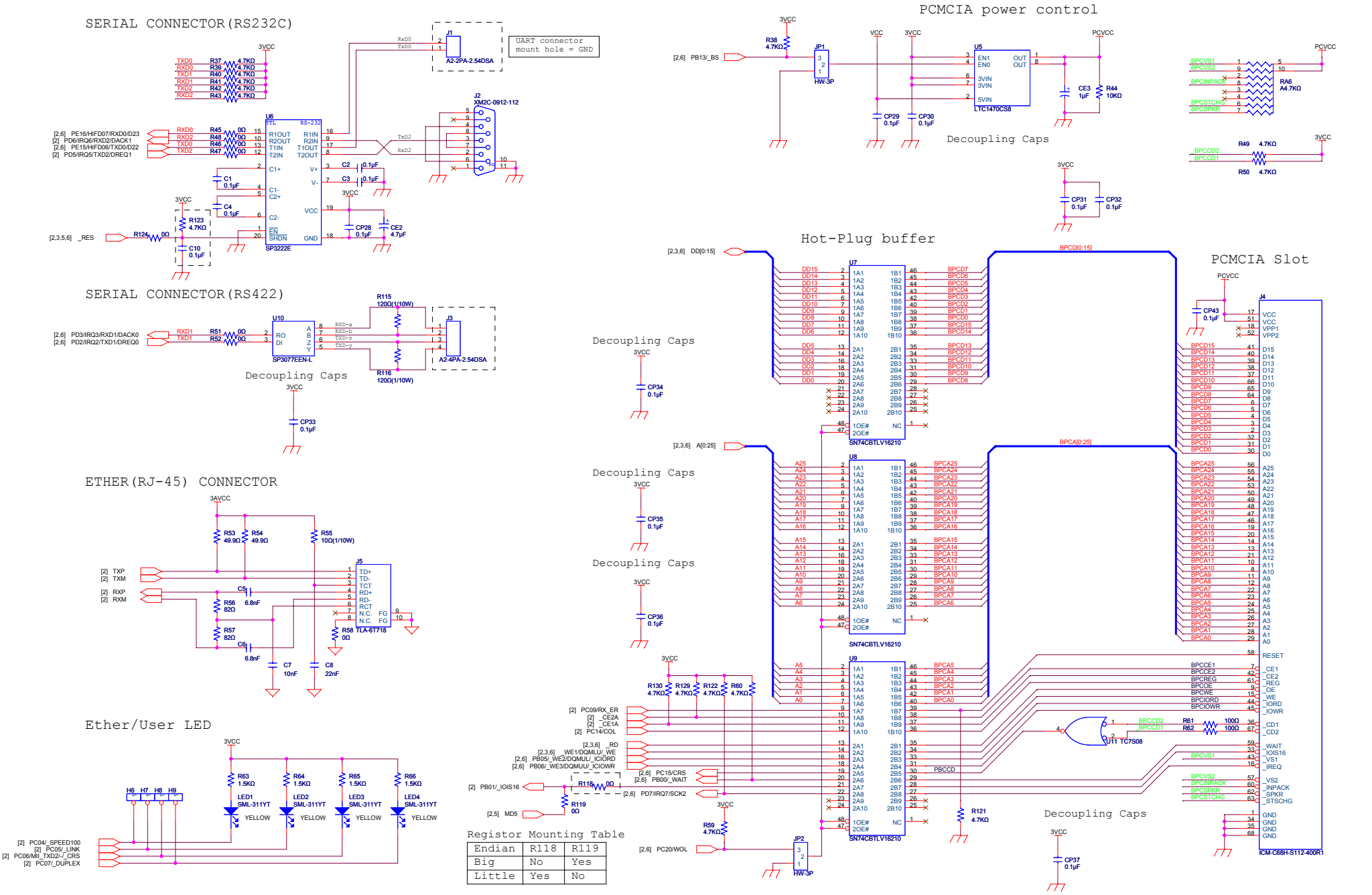


EEPROM



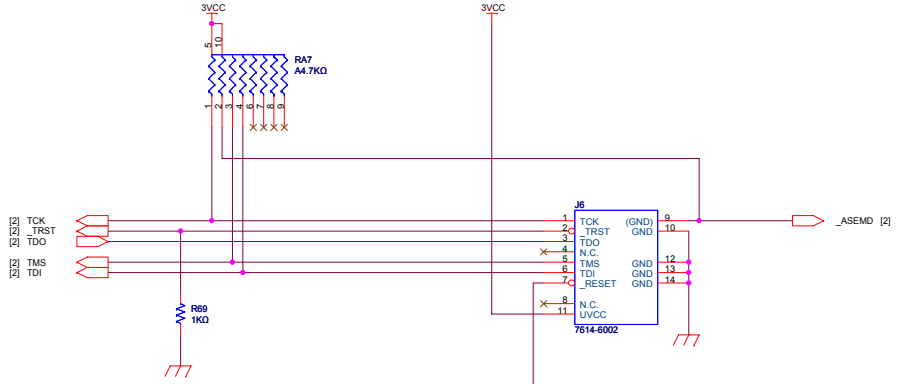
Decoupling Caps

CHANGE			RENESAS SOLUTIONS CORPORATION				M3A-HS19
			DRAWN	CHECKED	DESIGNED	APPROVED	FLASH MEMORY/SDRAM/EEPROM (3 / 7)
Ver.1.01		SCALE					DK30575-C
		DATE	08-08-19				

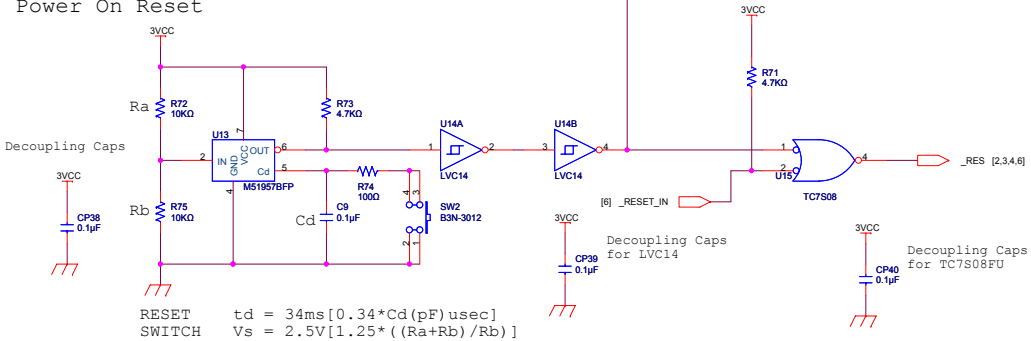


CHANGE		RENESAS SOLUTIONS CORPORATION				M3A-HS19
R63, R64, R65, R66 360R-> 1.5KR R55, R115, R116 1/16W -> 1/10W Ver.1.01	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	UART/ETHER/PCMCIA (4 / 7)
	DATE 08-08-19					DK30575-C

H-UDI INTERFACE

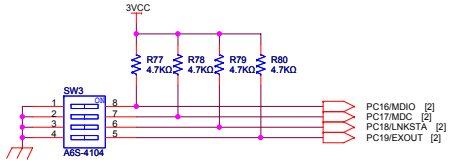


Power On Reset

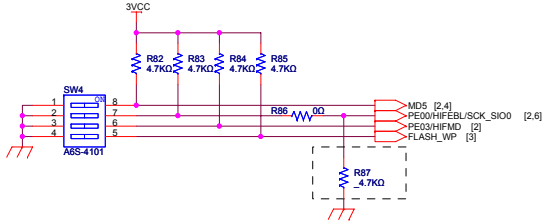


RESET SWITCH td = 34ms[0.34*Cd(pF)usec]
Vs = 2.5V[1.25*((Ra+Rb)/Rb)]

User Port



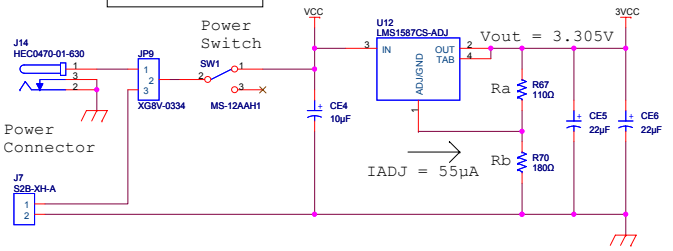
Mode Switch



1:ON BIG ENDIAN (MSB FIRST)
1:OFF LITTLE ENDIAN (LSB FIRST)
2:ON NOT HIF ACTIVE
2:OFF HIF ACTIVE
3:ON NORMAL BOOT
3:OFF HIF BOOT
4:ON FLASH WRITE PROTECT
4:OFF FLASH UNLOCK

5V TO 3.3V LINEAR REGULATOR

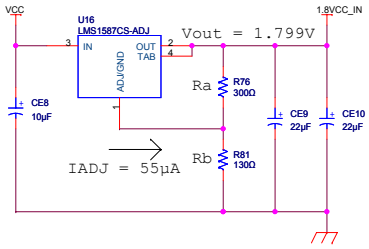
1-2 Power On
2-3 Power Off



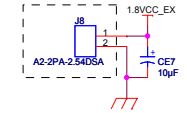
VOUT = VREF * (1 + Rb/Ra) + IADJ * (Rb)

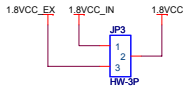
All regulator TABs are VOUT.

5V TO 1.8V LINEAR REGULATOR



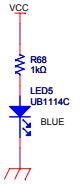
1.8V EXTERNAL





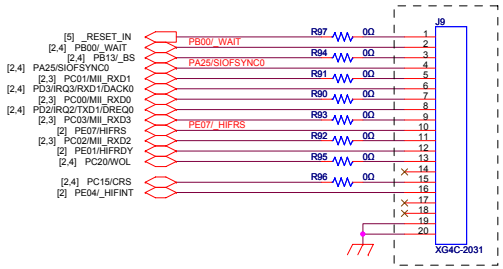
1-2 Fixed 1.8V
2-3 External 1.8V

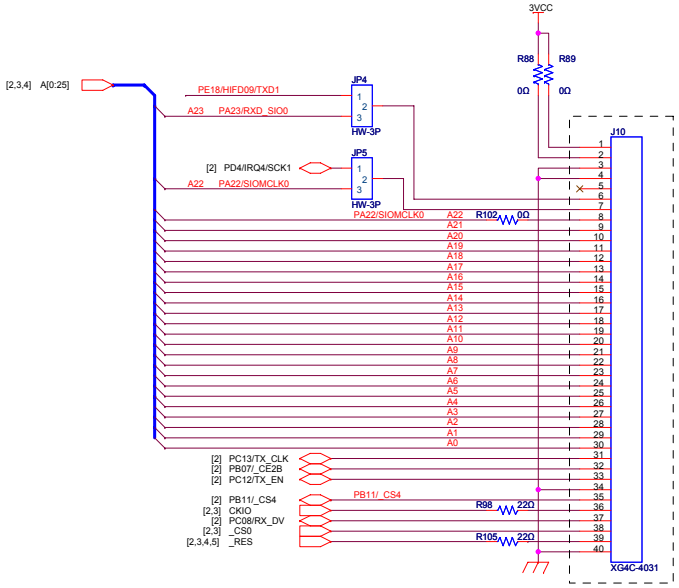
POWER LED VCC

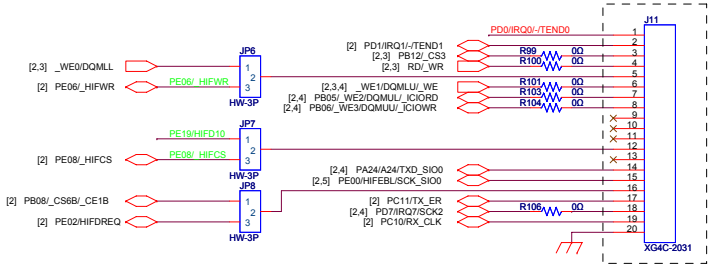


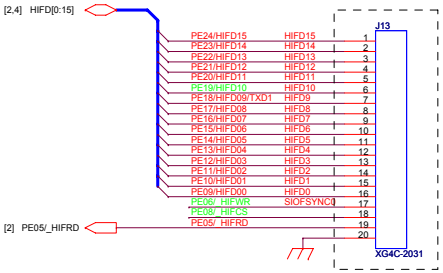
CHANGE					RENESAS SOLUTIONS CORPORATION	M3A-HS19
Ver.1.01	SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	H-UDI/RESET/POWER (5 / 7)
	DATE	08-08-19					DK30575-C

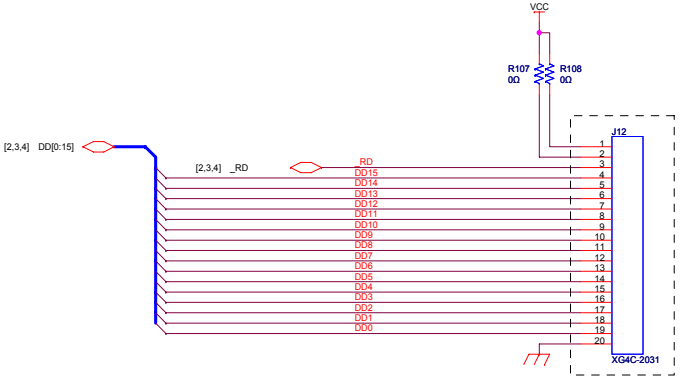
Extension Bus Connector



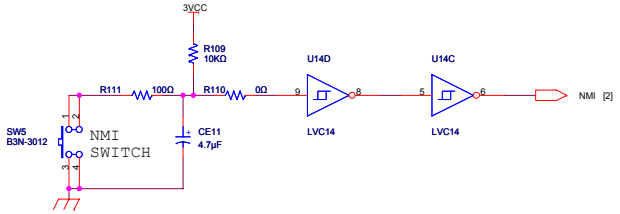




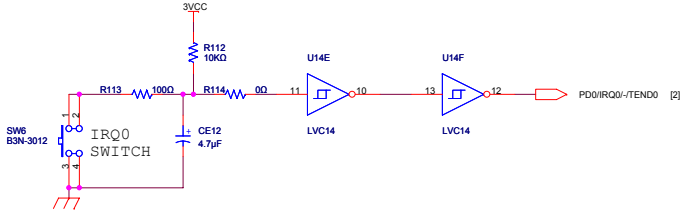




NMI SWITCH CIRCUIT

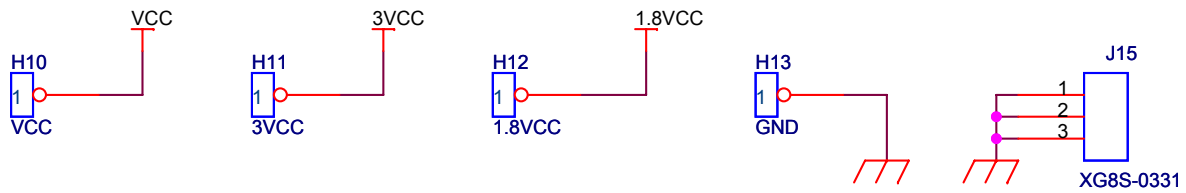


IRQ0 SWITCH CIRCUIT

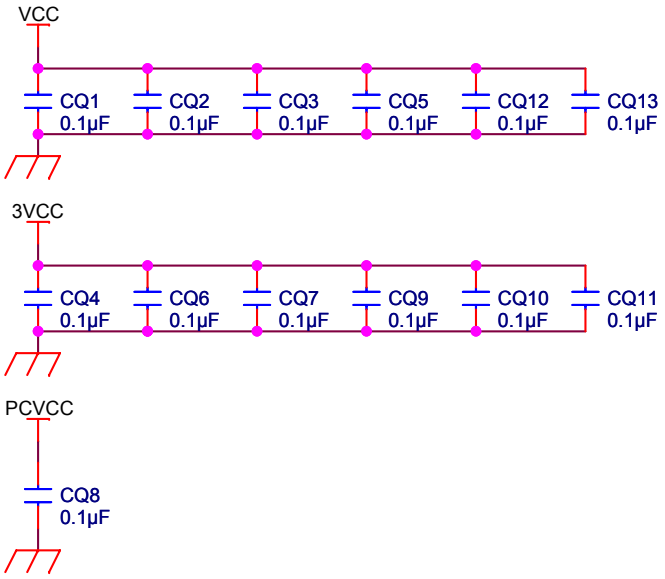


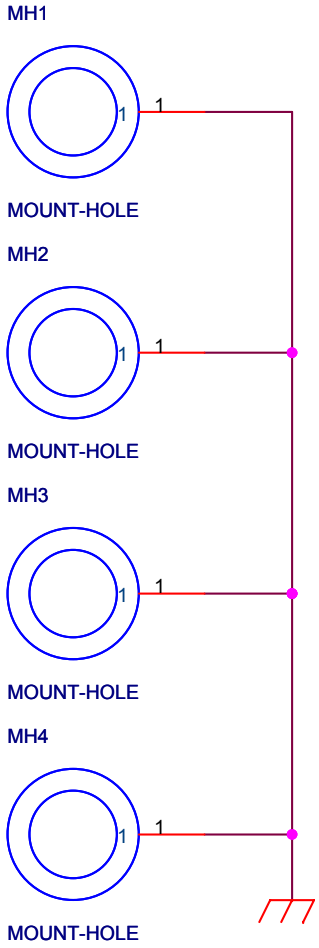
CHANGE	R98 0R -> 22R Ver.1.01		RENESAS SOLUTIONS CORPORATION		M3A-HS19
		SCALE	DRAWN	CHECKED / DESIGNED / APPROVED	BUS CONNECTORS/PUSH SW (6 / 7)
		DATE 08-08-19			DK30575-C

TEST PIN



AGND-GND





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		Page	Summary
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